EXHIBIT F

Exhibit Designated

HIGHLY CONFIDENTIAL ATTORNEYS' EYES ONLY

Under Stipulated Protective Order

EXHIBIT G

Exhibit Designated

HIGHLY CONFIDENTIAL ATTORNEYS' EYES ONLY

Under Stipulated Protective Order

EXHIBIT H

US005736850A

United States Patent [19]

Legal

[11] Patent Number: 5,736,850

[45] Date of Patent: Apr. 7, 1998

[54] **CONFIGURABLE PROBE CARD FOR AUTOMATIC TEST EQUIPMENT**

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[73] Assignee: **Teradyne, Inc.**, Boston, Mass.

[21] Appl. No.: **526,302**

[22] Filed: **Sep. 11, 1995**

[51] **Int. Cl.**[6] **G01R 31/02**

[52] **U.S. Cl.** **324/158.1**; 324/754

[58] **Field of Search** 324/754, 72.5, 324/158.1, 765

[56] **References Cited**

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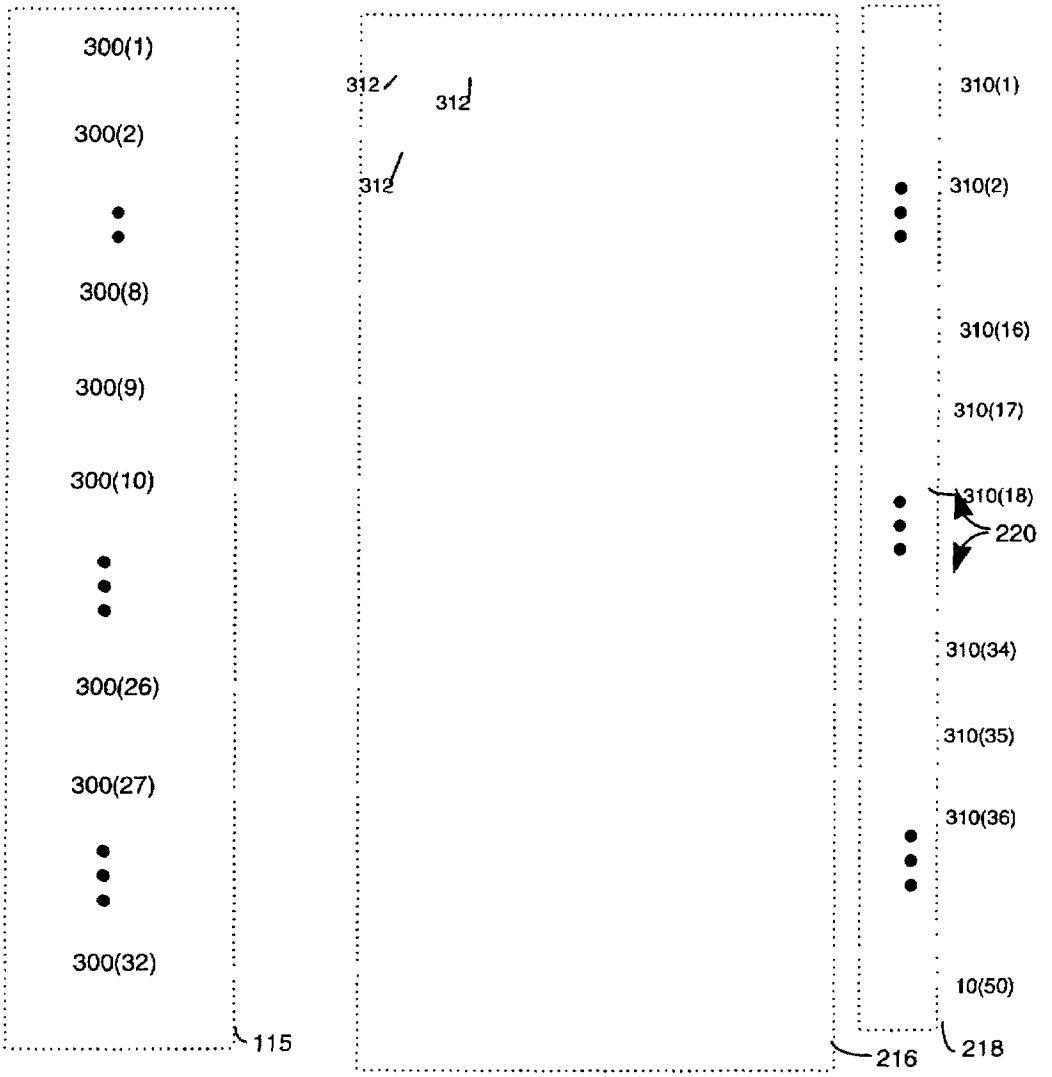
Primary Examiner—Ernest F. Karlsen
Assistant Examiner—Anh Phung
Attorney, Agent, or Firm—Edmund J. Walsh

[57] **ABSTRACT**

A configurable probe card for use with a tester for semiconductor devices. The probe is configurable so that the contact pattern during each touch down can be different. In this way, the number of devices being tested simultaneously can be maximized. The configurable probe card increases the utilization of the tester, thereby allowing increased throughput in the semiconductor manufacturing process or, alternatively, decreasing the overall cost of testing each device.

11 Claims, 4 Drawing Sheets



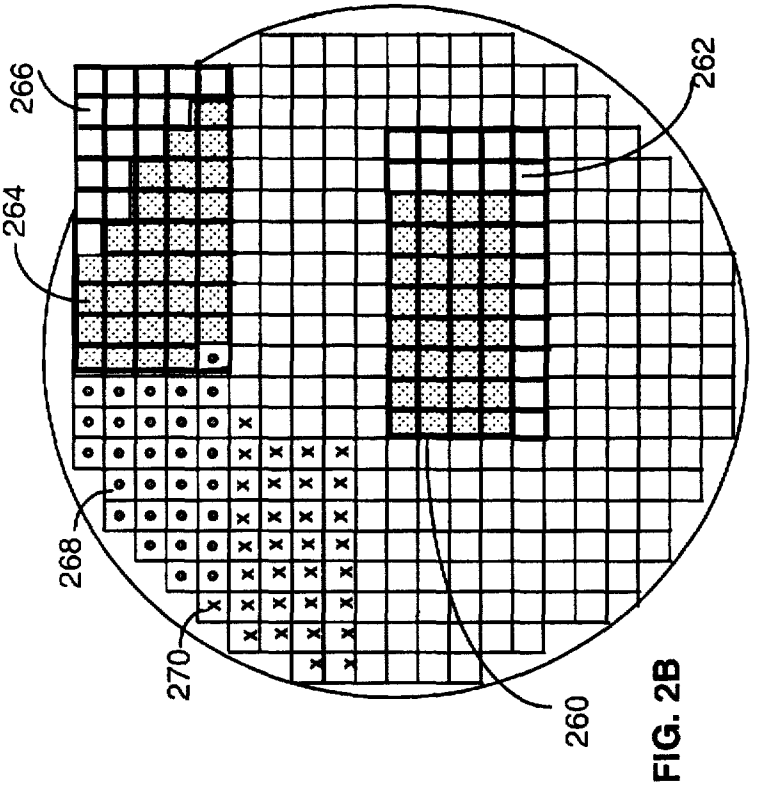


FIG. 2B

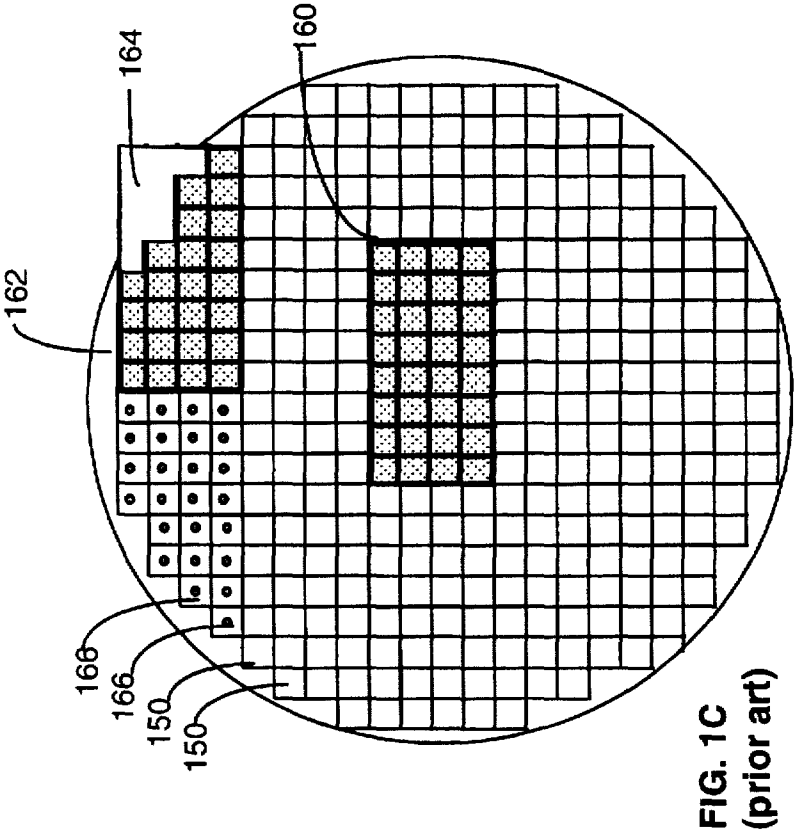


FIG. 1C
(prior art)

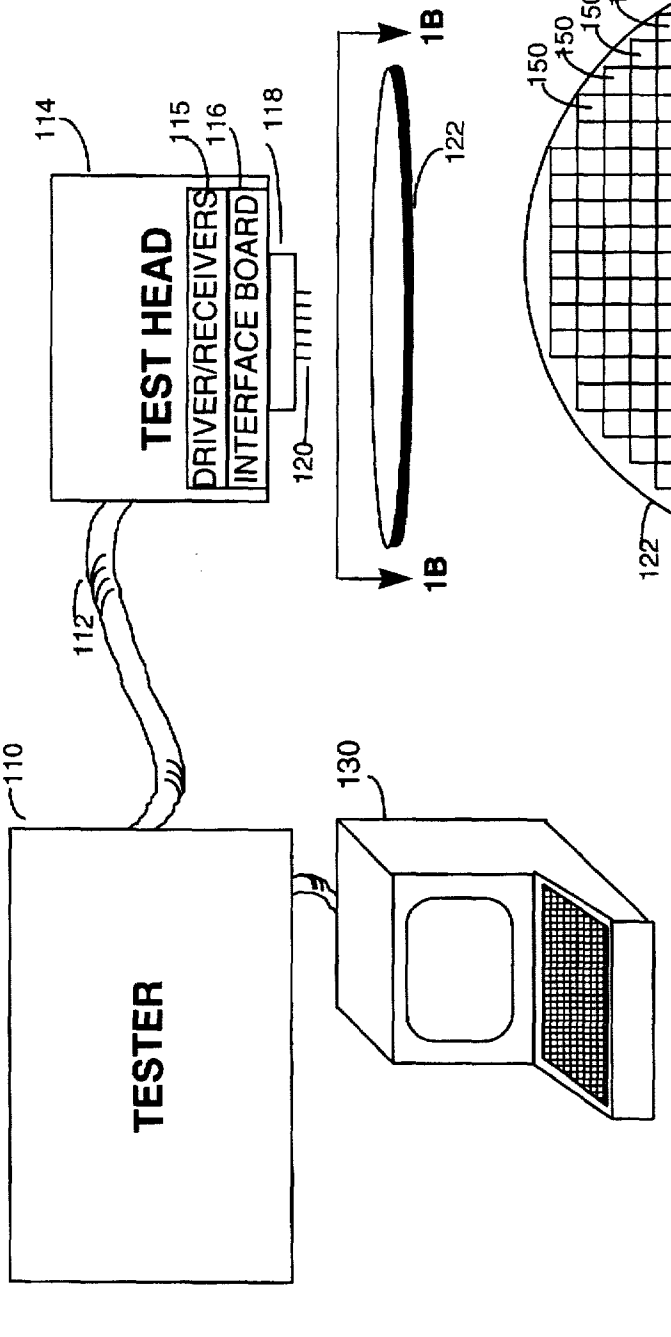


FIG. 1A
(prior art)

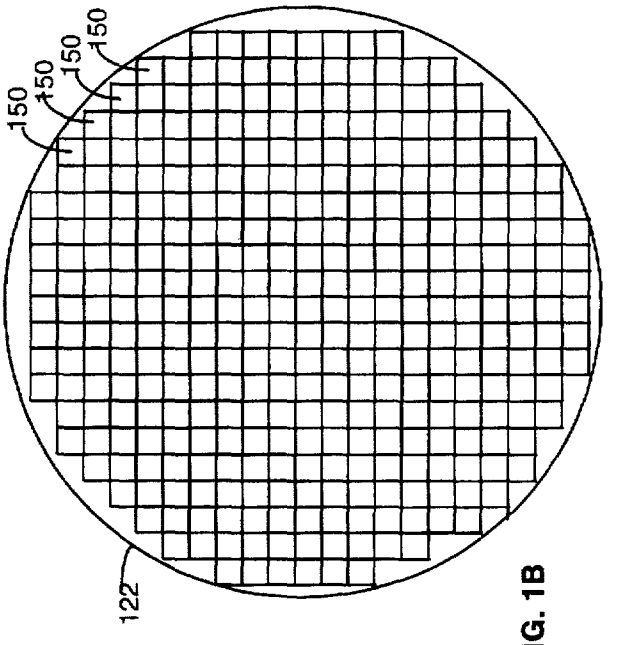


FIG. 1B

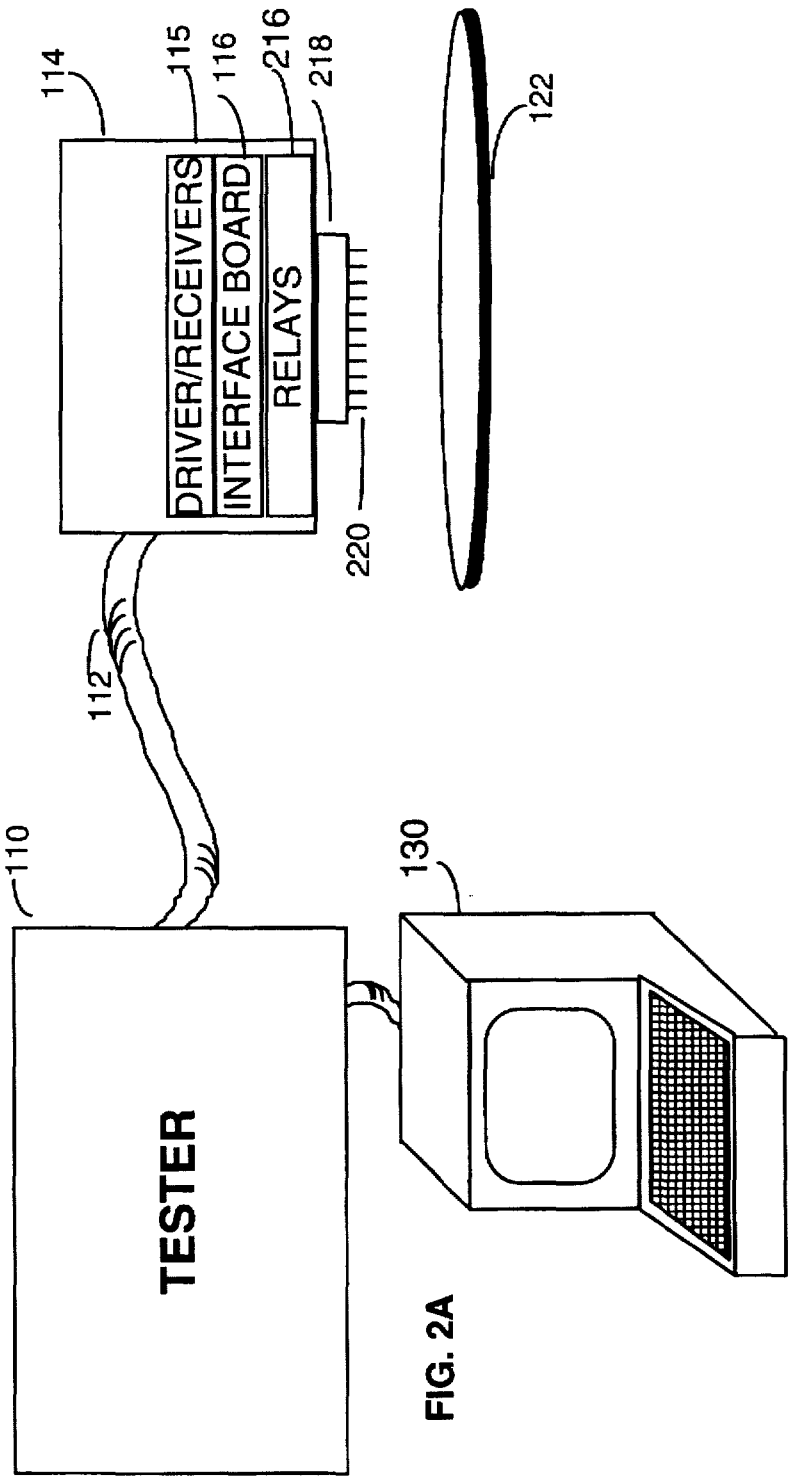

114
115
116
216
218
122
DRIVER/RECEIVERS
INTERFACE BOARD
RELAYS
220
112
110
130
TESTER

FIG. 2A

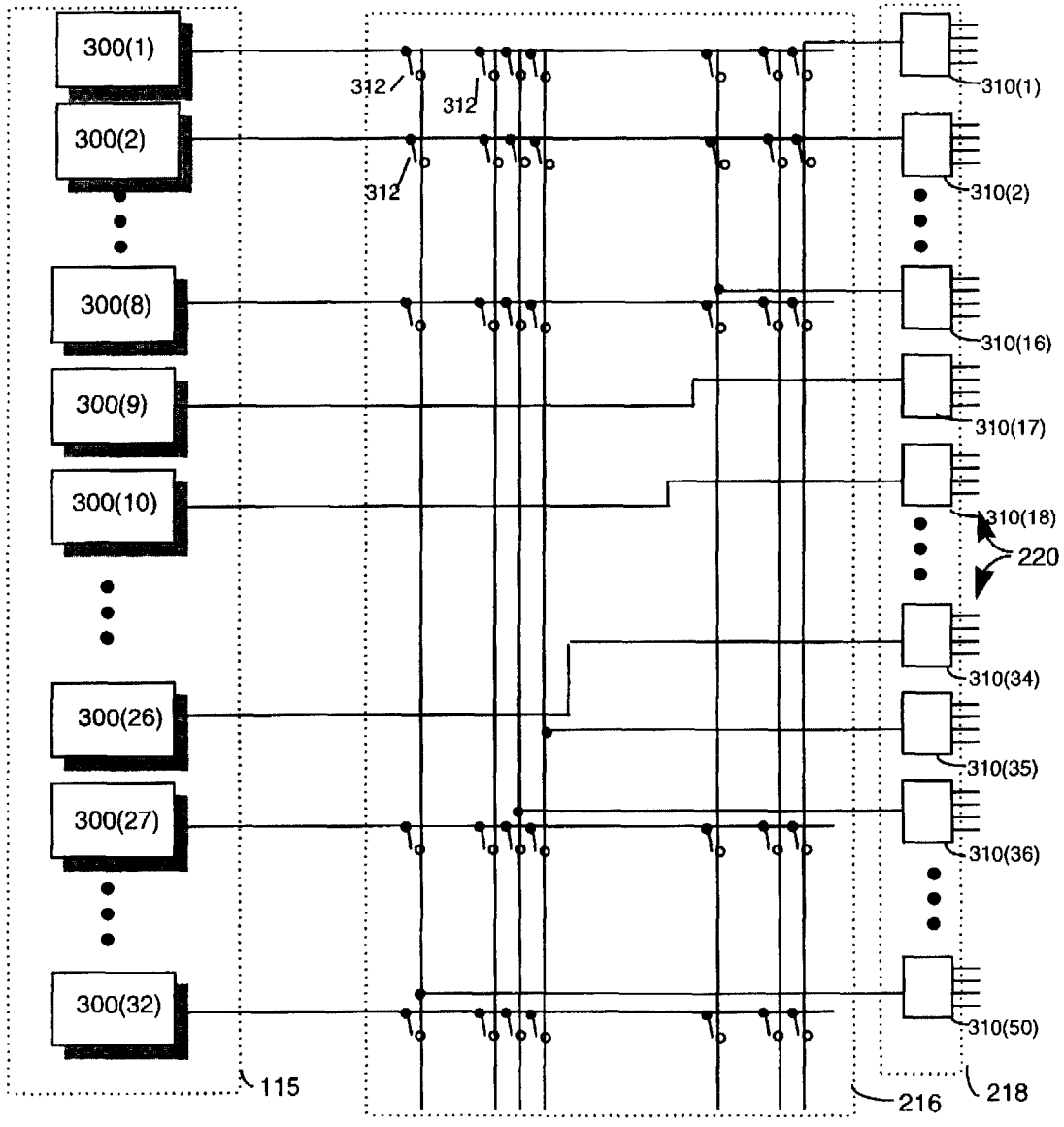

300(1)
300(2)
300(8)
300(9)
300(10)
300(26)
300(27)
300(32)
312
312
312
310(1)
310(2)
310(16)
310(17)
310(18)
220
310(34)
310(35)
310(36)
310(50)
115
216
218

FIG. 3

CONFIGURABLE PROBE CARD FOR AUTOMATIC TEST EQUIPMENT

This invention relates generally to automatic test equipment and more specifically to automatic test equipment used in the testing of semiconductor devices.

Semiconductor devices are generally tested at least once during their manufacture. Testing is used to identify and eliminate faulty components as early as possible during the manufacturing process. In this way, the cost of processing faulty parts is significantly reduced.

Semiconductor devices contain a die or "chip" of semiconductor material and some packaging material to provide mechanical support for the die and to allow electrical connections to be made to the die. Because the cost of packaging is relatively high, it is desirable that any defective dies be sorted out before packaging.

The semiconductor dies are generally made on silicon wafers. Wafers used today are typically 8 inches in diameter, though 12 inch diameter wafers are under development and are expected to be available soon. Many semiconductor dies are formed on a single wafer. The exact number depends on the size of the wafer and the size of the die, though several hundred to over a thousand die might be formed on one wafer. Testing of the dies is generally performed while they are still a part of the wafer.

Testing of semiconductor components is typically accomplished using very powerful automatic test equipment. The test equipment, called generally a "tester," is capable of generating numerous test signals and measuring responses. The generated signals are precisely controlled and the responses are very accurately measured. In this way, the tester can make a very accurate determination of whether a semiconductor die is functioning properly. Examples of such testers are the J995 and the J971 sold by Teradyne, Inc. of Agoura Hills, Calif., USA.

To test dies still on a wafer, a mechanism to make electrical contact to the individual dies must be used. A typical arrangement includes a probe card. Generally, the probe card has numerous individual probe wires in a pattern designed to make contact with contact pads on the die. However, other contact mechanisms are used in probe cards to make contact to many points. For example, some probe cards use flexible membranes with conductive portions on them which are pushed down onto the die.

The probe card is connected to a test head. The test head contains electronic circuitry to drive test signals and receive responses. To achieve high testing accuracy, it is necessary that this driver/receiver circuitry be as close as possible to the semiconductor die being tested. For that reason, it is often placed in a test head, allowing it to be separated from other electronic circuitry in the tester and placed closer to the semiconductor device.

During testing, the wafer is held in a device called prober. The prober is attached to the test head. The prober moves the wafer around to present different dies to the probe card. The tester runs through a test program to test the die presented to it. This test program is repeated each time a die is presented to the tester. In this way, every die on the wafer can be tested.

In some instances, one die is tested at a time. However, all of the dies on a wafer are usually the same. It is therefore possible that multiple dies be tested at one time with one run through the test program in the tester. When multiple dies are tested simultaneously, the probe wires on the probe card are divided into test "sites." Each site includes the probe wires for one die. The signals provided for each site are the same.

Testers for semiconductor memories are often configured with multiple sites. Thirty-two test sites in a tester is not

uncommon in a memory tester. There must be separate driver and/or receiver ("driver/receiver") circuitry for each signal probe wire in each site, but other circuitry in the tester can be used to generate signals for multiple test sites. In this way, the cost of the test equipment on a per wafer basis is reduced. Also, the throughput of the test equipment can be increased.

Probe card technology is lagging slightly behind tester technology. Current probe cards generally test a maximum of sixteen sites at once, but larger probe cards are becoming available.

Throughput is very important in semiconductor processing for two reasons. First, the cost of the processing equipment is very high. On the other hand, semiconductor components sell for a relatively low price. Therefore, semiconductor manufacturers must be able to amortize the high cost of processing equipment over a very large number of semiconductor devices processed by that equipment. Second, semiconductor components must be manufactured in clean rooms so that dust or other contaminants not ruin the semiconductor components. Clean rooms are expensive to build and generally have limited floor space. The amount of equipment that can be placed in a clean room is limited. Therefore, each piece of equipment must process many semiconductor devices.

SUMMARY OF THE INVENTION

With the foregoing background in mind, it is an object of the invention to increase the throughput of a tester having multiple test sites.

It is also an object to reduce the cost of testing semiconductor memory chips.

The foregoing and other objects are achieved in a tester having a configurable probe card. The tester generates signals for multiple test sites. The probe card contains probe wires or other contact mechanisms for multiple test sites. However, the probe card has contact mechanisms for more test sites than the tester can generate signals for. A switch array is placed between the tester circuitry and the contact points to change which of the test sites on the probe card are connected to the tester circuitry.

In operation, the switch array is used to select different configurations of test sites on the probe card. The configurations for successive runs of the test program are selected based on the position on the wafer of the dies being tested. In this way, the total number of test runs is reduced and throughput increases.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1A is sketch illustrating a prior art test set up;

FIG. 1B is a sketch illustrating the surface of a semiconductor wafer;

FIG. 1C is a sketch illustrating how multiple test sites of the prior art system of FIG. 1A might be used to test multiple dies on the wafer shown in FIG. 1B;

FIG. 2A is a sketch illustrating a test set up according to the invention;

FIG. 2B is a sketch illustrating how multiple test sites of the invention of FIG. 2A might be used to test multiple dies on the wafer shown in FIG. 1B; and

FIG. 3 is a schematic diagram showing greater detail of a preferred configuration of the relays of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1A shows a tester main frame **110** as in the prior art. The tester main frame **110** contains the circuitry and software programming which specifies test signals and expected results.

A test head **114** is connected to the tester main frame **110**. Here, the connection is shown to be made through a cable **112**. Such a configuration is shown as representative of the art. However, testers exist in which the test head is incorporated into the same physical structure as the tester main frame. The exact configuration is not important to the invention.

Test head **114** contains numerous drivers and receivers **115**. There is generally one driver/receiver for each signal to be generated or measured.

The driver/receivers are connected through interface board **116** to probe card **118**. Interface board **116** provides a convenient means for mechanical interconnection and might also contain some components for signal conditioning or other functions. The exact interconnection of the driver/receivers **115** to probe card **118** is not important to the invention.

Probe card **118** contains numerous probe wires **120** which are grouped into a plurality of identical test sites. The probe wires in each test site **120** make contact to one die on wafer **122**. In the example given herein, there are **32** test sites.

Probe card **118** can be a specially manufactured printed circuit type board with physical wire type probes extending from it. However, as used herein, the term "probe card" is not limited to a printed circuit board. It is intended to encompass any structure used to hold conductive probes. Likewise, the term "probe wires" is not limited to a wire. It is intended to encompass any method of making electrical connection to multiple individual spots on a die, such as a conductive membrane.

Probe wires make contact with die on a wafer **122**. As described above, the wafer is held and positioned in a prober, which is not shown.

FIG. 1B shows the surface of wafer **122**. There are numerous dies **150** on the surface of wafer **122**. During one pass through the test program, the probe wires (**120**, FIG. 1) of the tester will make contact with several of the dies **150**. In the case where there are **32** test sites, the probe wires can make contact with up to thirty-two dies.

FIG. 1C shows a contact pattern **160** in which **32** dies within the contact pattern are simultaneously contacted. Contact pattern **160** is in the center of the wafer.

However, FIG. 1C also shows a contact pattern **162** in which only twenty-four dies are simultaneously contacted. The sites in region **164** do not contact any dies **150** on wafer **122** because they extend beyond the edge of wafer **122**.

To test all of the cells in the top four rows of wafer **122**, a second pass through the test program is necessary. The dies **166** marked with a circle are tested in this second pass. There are **25** such dies in the second pass.

We have recognized that the configuration of the test sites on probe card **118** limits the throughput of the test process. In particular, in two passes through the test program, only a total of fifty-one dies can be tested. The tester is, however, capable of generating test signals for sixty-four dies. Therefore, the tester is only about 80% utilized in those two passes. Stated another way, the tester could have tested 20% more parts in the same time. Providing a tester with a much greater utilization would increase the throughput of the manufacturing operation.

FIG. 2A shows an adaptation to the test system which would allow greater utilization of the tester. In place of probe card **118**, probe card **218** is used. Probe card **218** has more probe wires **220** than probe card **118**. The probe wires are organized into more test sites. For the examples given herein, probe card **218** contains fifty test sites.

However, tester **110** is capable of generating test signals for fewer test sites. Some or all of the test sites on probe card **218** are connected to tester **110** through relay matrix **216**. In this way, for each pass through the test program, the pattern of test sites can be different. This flexibility allows greater utilization of the tester.

FIG. 2B shows a contact pattern **260**. Contact pattern **260** is in the center of wafer **122**. It has thirty-two active test sites, just like contact pattern **160** (FIG. 1C). Contact pattern **260** also includes eighteen test sites in region **262**. Because tester **110** is only capable of generating test signals for thirty-two test sites, the test sites on probe card **218** in region **262** do not provide test signals. They are inactive and are not connected to tester **110** through relays **216**.

The advantage of the invention is apparent from contact pattern **264**. Contact pattern **264** is at the edge of a wafer **122**. Nonetheless, thirty-two test sites are active in contact pattern **264**. Eighteen test sites in region **266** are inactive. However, tester **110** is fully utilized generating test signals for the test sites in contact region **264**. Therefore, there is no loss in tester utilization.

A second pass through the test program can be used to test the dies **268** marked with circles. Again, thirty-two dies are tested in the second pass, fully utilizing the tester. In a third pass, thirty-two dies **270** marked with an X can be tested, again fully utilizing the tester.

In each case, the pattern of active test sites in patterns **264**, **268** and **270** is slightly different. Thus, it is said that probe card **218** is "configurable." The total number of test sites on card **218** is fixed, but the ones used at any pass through the test program can be different to get maximum utilization of tester **110**. The active test sites are selected through activation of specific relays **216**.

FIG. **3** shows the circuitry in test head **114** in greater detail. Driver/receiver board **115** is shown to contain thirty-two groups of driver/receiver circuits **300(1) . . . 300(32)**. Each of the groups **300(1) . . . 300(32)** contains the drivers and receivers needed to generate test signals for one of the test sites **310(1) . . . 310(50)**.

Interface board **116** is not explicitly shown in FIG. **3**, as this board provides largely mechanical interfacing and does not affect the signal flow shown in FIG. **3**.

Relay board **216** contains a plurality of relays **312**. Each of the relays **312** can be actuated to connect one of the groups of driver receivers to one of the test sites. It will be appreciated that each of the test sites contains a plurality of probe wires. Thus, to switch a group of driver/receiver circuits to a test site, a plurality of connections must be made. Thus, relays **312** actually represent a plurality of relays in parallel, providing independent signal paths for each of the probe wires **220** in a test site.

Relays **312** may be traditional mechanical type relays. Alternatively, they could be solid state switches or other similar structure. Such relays or switches have control inputs, which are not shown in FIG. **3** for clarity. However, the control inputs to relays **312** are connected back through cable **112** to computer **130**. As in the prior art, computer **130** controls the overall test process, including the interaction between tester **110** and the prober holding wafer **122**. Thus, computer **130** is programmed to actuate appropriate ones of

the relays **312** to provide the desired contact pattern for each pass through the test program in tester **110**.

In the embodiment of FIG. **3**, only some groups of driver/receiver circuits are connected to test sites through relays **312**. Groups **300(9)** . . . **300(26)** are wired directly to test sites **310(17)** . . . **310(34)**. Test sites **310(17)** . . . **310(34)** are preferably in the center of probe card **218**. The remaining test sites, **310(1)** . . . **310(16)** and **310(36)** . . . **310(50)**, can be connected to one of the remaining groups **300(1)** . . . **300(8)** or **300(27)** . . . **300(32)**.

Having a portion of the test sites wired directly to groups of driver/receiver circuits slightly reduces the number of contact patterns which are possible. However, as some of the test sites in the center of probe card **220** must be active if there are to be thirty-two active test sites, this restriction is not significant. This restriction provides the benefit of reducing the total number of relays **312** required.

The number of test sites connected to groups of driver/receiver circuits through relays **312** is not important to the invention. All or some fraction of the test sites might be connected through the relays.

In use, a probe card will be made for each type of device that must be tested since each device requires its own layout of probe wires. For that reason, test head **114** is made to accept many different sizes and configurations of probe cards.

The size of the configurable probe card may also be different for different types of devices. The size and shape of the configurable probe card are selected to give high tester utilization without unnecessarily increasing cost. The required size and shape will depend of the layout of dies **150** on wafer **122**. For example, one layout might achieve a very high utilization with a configurable probe card having **40** test sites arranged in a 5×8 rectangular array. To test devices on such a wafer, a 5×8 rectangular array might be adequate. As another example, a wafer with a different layout might result in an unacceptable utilization with the **40** site probe card. On the other hand, that wafer might achieve a very high utilization with a fifty site probe card, with the sites arranged in a 5×10 array. Such a probe card would preferably be used to test that wafer.

In situations where a probe card with fewer test sites can be used while still achieving the same, or almost the same, utilization as a larger probe card, the smaller probe card would be preferred. The smaller probe card would be less expensive and therefore more desirable.

In a factory where semiconductor devices are manufactured, a specific tester **110** is usually dedicated to test a certain type of components for an extended period of time. The tester and associated test head, computer and prober are configured for that type of device. As part of that configuration process, the size and configuration of the probe card would be selected. Also, the contact pattern for the active test sites would be selected for each pass through the test program. One pass through the test program is sometimes called a "touchdown" because, for each pass through the test program the wafer **122** is brought into contact with probe wires **220**.

The contact size and configuration of the probe card might be determined by a computer program running on computer **130** or some other computer, which need not be connected to tester **110**. Such a program would accept as inputs the layout of dies **150** on wafer **122** and the total number of active test sites test head **114** could support. For various size configurable probe cards, the computer program would try various contact patterns at different touchdowns and construct a set of contact patterns which allowed each die **150** to be tested. For each size of configurable probe card, the set of contact patterns which required the minimum number of touchdowns would be saved.

This processing would be repeated for each size of configurable probe card. The smallest configurable probe card which resulted in adequate tester utilization would be selected. The selected contact pattern for each touchdown would be saved for use by computer **130** in controlling relays **312** during various passes through the test program.

In this way, high tester utilization is achieved with relatively modest added cost. More devices can be tested in a fixed period of time, thereby reducing the total cost of testing the components.

Having described one embodiment, numerous alternative embodiments or variations might be made. For example, the configurable probe cards were described to be rectangular arrays of test sites. No such configuration is necessary. For some wafers, more efficient utilization might be obtained by staggering the number of test sites in each row to match the layout of dies near the edge of the wafer.

Also, it was described that control inputs for relays **312** were provided from computer **130**. The control inputs might come from any computer involved in the testing operation. For example, probers generally have computers which could generate the required control signals.

Also, it was described that relays **312** are included on a separate board. The relays could be included as part of interface board **116**. Alternatively, the relays might be included on driver/receiver boards **115**. As another variation, it is not necessary that the relays be inserted into test head **114**, though such an arrangement is desirable because it allows the relays to be placed near both driver receivers **115** and the devices under test.

As another example of possible variations, it should be noted that the switching array of FIG. **3** is illustrative only. A full switching matrix could be used to allow any test site to be connected to any group of driver/receiver circuits. Alternatively, certain driver/receiver circuits might be switched to only one of a few test sites. The exact switching arrangement is preferably selected to use as few relays as possible to generate all required contact patterns.

Therefore, the invention should be limited only by the spirit and scope of the appended claims.

What is claimed is:

1. Automatic test equipment for use in testing semiconductor components on a wafer, each wafer containing a plurality of dies disposed in a predetermined pattern, comprising:

a) a first plurality of groups of test signal circuits, each group of test signal circuits for driving and receiving test signals for one die on the wafer;

b) a contact device having a second plurality of groups of contact points, each group of contact points for contacting test points on one die on the wafer, the second plurality being larger than the first plurality; and

c) a matrix of a third plurality of switchable elements connected between the first plurality of groups of test signal circuits and the second plurality of groups of contact points, each switchable element connecting one of the groups of test signal circuits to one of the groups of contact points contacting test points on the plurality of dies disposed in the predetermined pattern.

2. The automatic test equipment of claim **1** wherein the contact device comprises a probe card.

3. The automatic test equipment of claim 1 additionally comprising a test head, wherein the first plurality of groups of test signal circuits comprise driver/receiver circuits in the test head.

4. The automatic test equipment of claim 3 wherein the matrix of switchable elements is located within the test head.

5. The automatic test equipment of claim 1 wherein the third plurality is less than the first plurality and the automatic test equipment additionally comprises signal paths between a portion of the first plurality of groups of test signal circuits and a portion of the second plurality of groups of contact points, such paths being separate from the switchable elements.

6. The automatic test equipment of claim 1 additionally comprising means for actuating selected ones of the switchable elements while dies on the wafer are being tested, thereby configuring the contact device such that the groups of contact points contact test points on other pluralities of dies disposed in different predetermined patterns.

7. The automatic test apparatus of claim 6 wherein the means for actuating comprises a computer work station connected to the automatic test equipment.

8. A process for manufacturing semiconductor components including a step of testing the components while on a semiconductor wafer, the step of testing comprising the steps of:

a) connecting a first set of test sites on a probing device to electronic circuitry for generating and receiving test signals;

b) bringing the probing device and the semiconductor wafer into contact such that the first set of test sites contacts a first plurality of components on the semiconductor wafer;

c) testing the first plurality of components on the wafer;

d) connecting the electronic circuitry to a second set of test sites on the probing device, at least a portion of the test sites in the second set not being in the first set; and

e) bringing the probing device and the semiconductor wafer into contact such that the second set of test sites contacts a second plurality of components on the semiconductor wafer; and

f) testing the second plurality of components on the wafer, wherein the electronic circuitry is only capable of generating and receiving test signals for less than the total number of test sites in the first set and the second set.

9. The process of claim 8 wherein the first plurality of components is different from the second plurality of components.

10. The process of claim 8 wherein the semiconductor components are semiconductor memories.

11. The process of claim 8 wherein the steps of connecting comprise actuating switches to connect a first plurality of circuits, each of the circuits generating test signals to test a semiconductor component, to selected ones of a second plurality of test sites in the probing device, the second plurality being larger than the first plurality.

* * * * *

EXHIBIT I

US006366112B1

(12) **United States Patent**
Doherty et al.

(10) **Patent No.: US 6,366,112 B1**
(45) **Date of Patent: *Apr. 2, 2002**

(54) **PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/973,509**

(22) Filed: **Oct. 9, 2001**

Related U.S. Application Data

(62) Division of application No. 09/420,256, filed on Oct. 18, 1999, now Pat. No. 6,300,786, which is a division of application No. 09/075,691, filed on May 11, 1998, now Pat. No. 6,246,250.

(51) **Int. Cl.**[7] **G01R 31/26**; G01R 31/02

(52) **U.S. Cl.** **324/765**; 324/754; 324/755; 324/757; 324/758; 324/158.1

(58) **Field of Search** 324/765, 754, 324/755, 757, 758, 158.1

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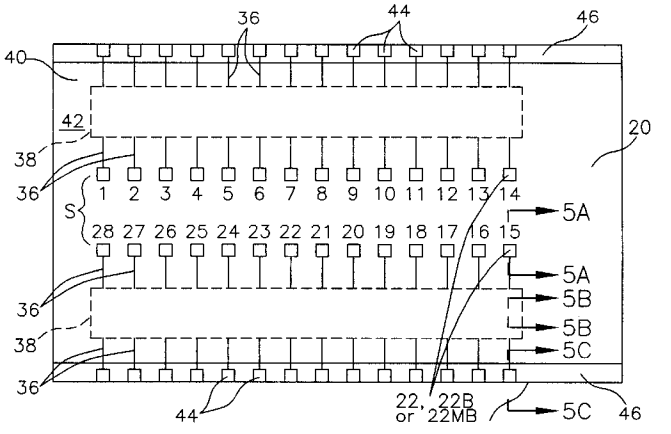
(57) **ABSTRACT**

A probe card for testing semiconductor wafers includes probe card contacts for electrically engaging die contacts on the wafer. The probe card also includes an on board multiplex circuit adapted to fan out and selectively transmit test signals from a tester to the probe card contacts. The multiplex circuit expands tester resources by allowing test signals to be written to multiple dice in parallel. Reading of the dice can be performed in groups up to the limit of the tester resources. In addition to expanding tester resources, the multiplex circuit maintains the individuality of each die, and permits defective dice to be electrically disconnected.

21 Claims, 7 Drawing Sheets



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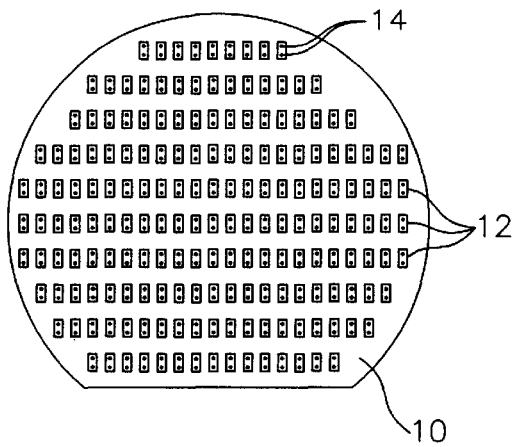


FIGURE 1
(PRIOR ART)

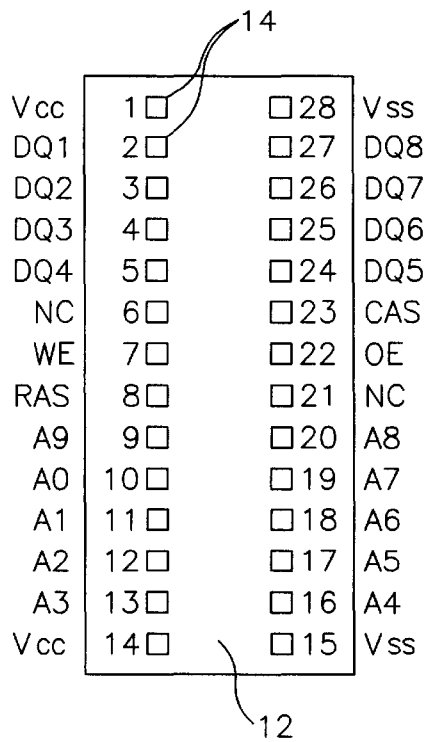


FIGURE 2
(PRIOR ART)

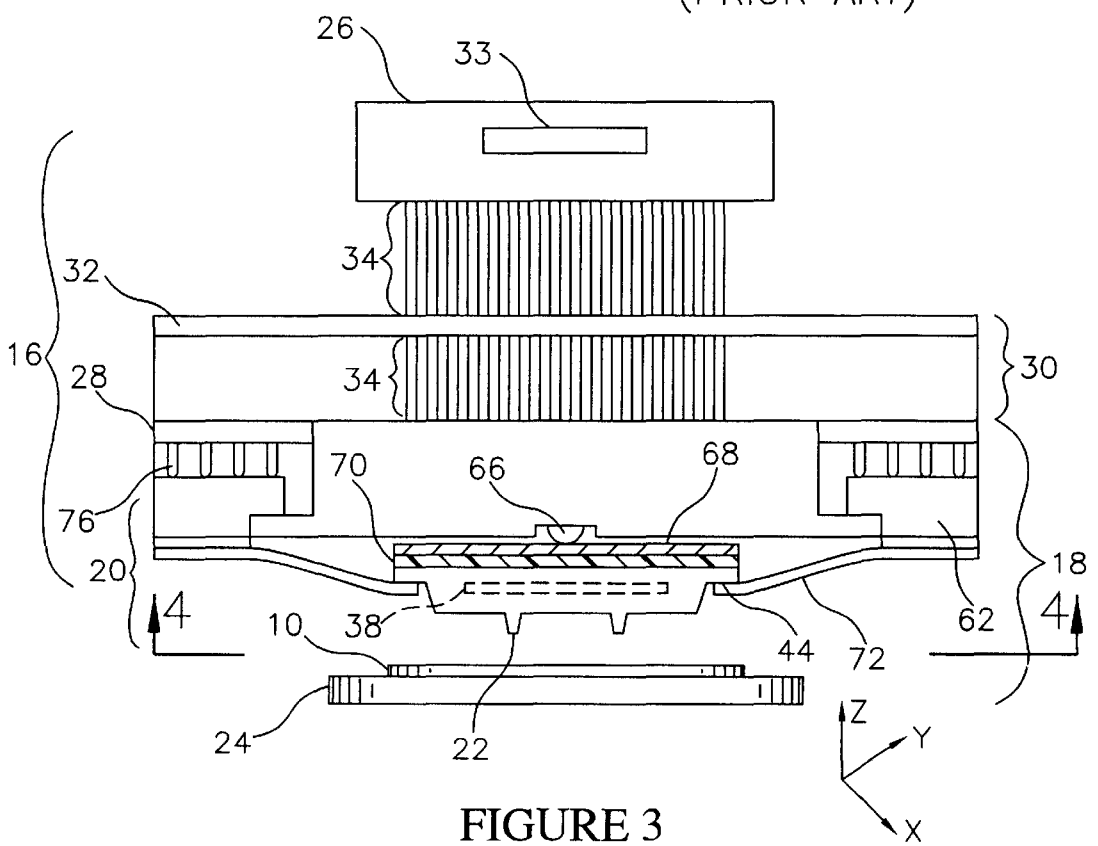


FIGURE 3

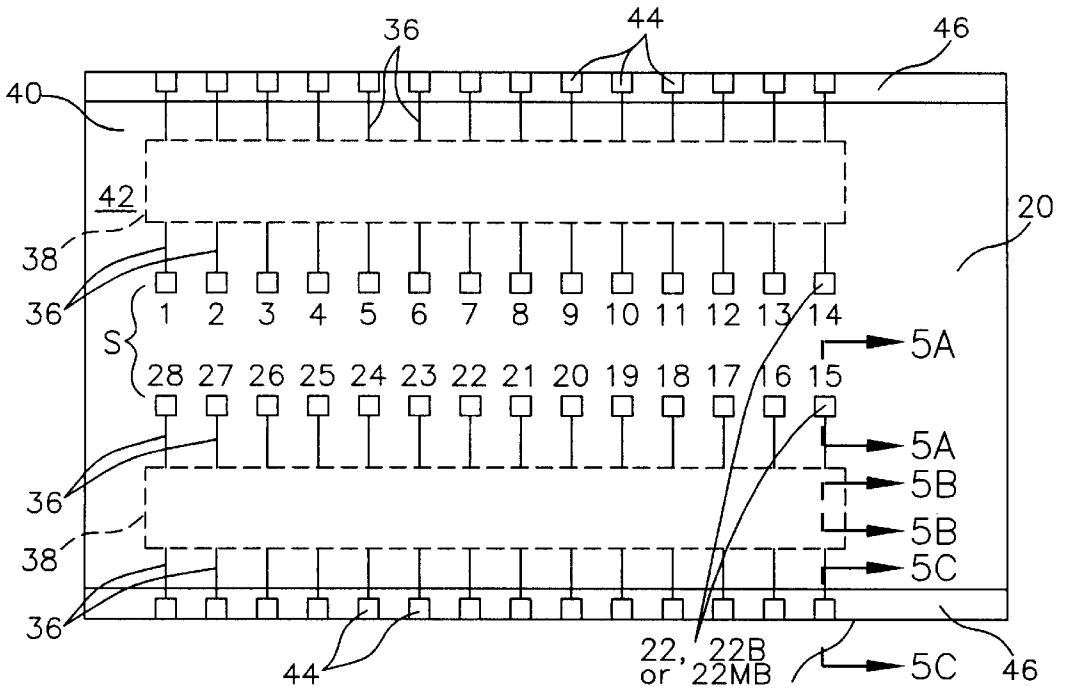


FIGURE 4

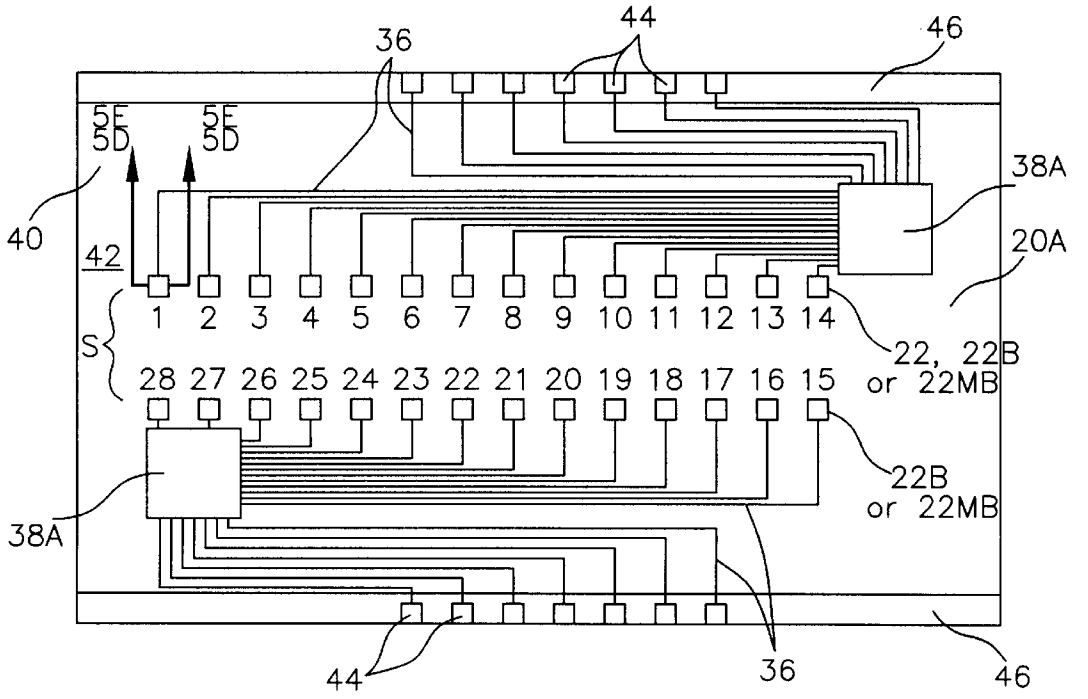


FIGURE 4A

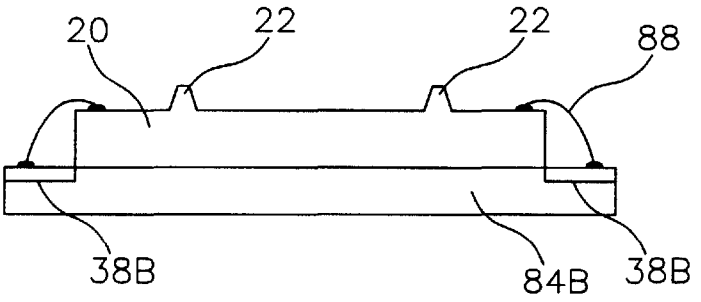


FIGURE 4B

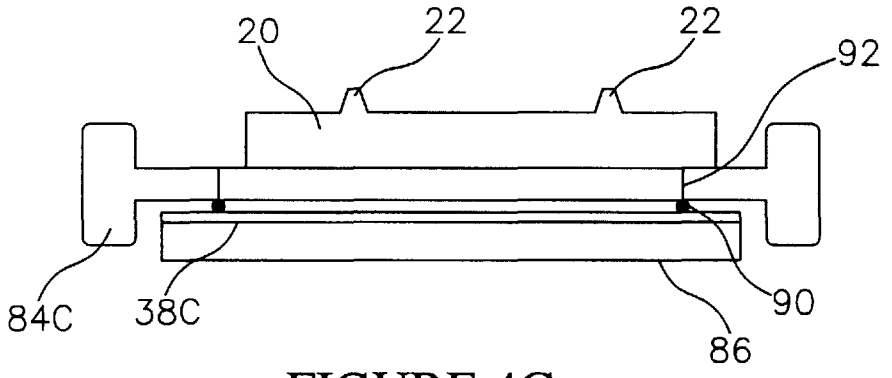


FIGURE 4C

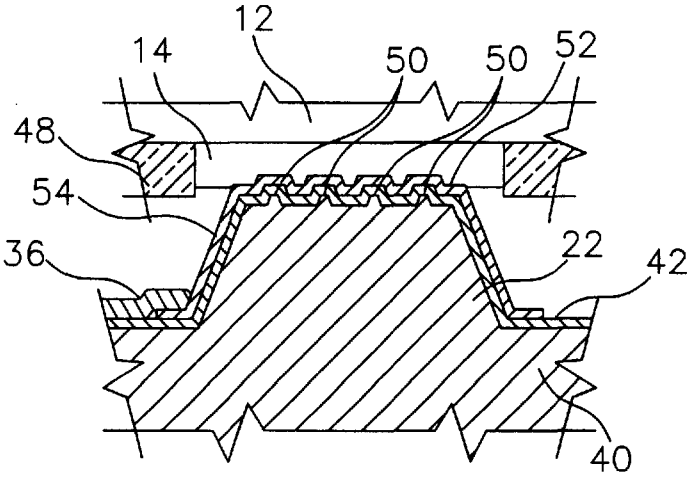


FIGURE 5A

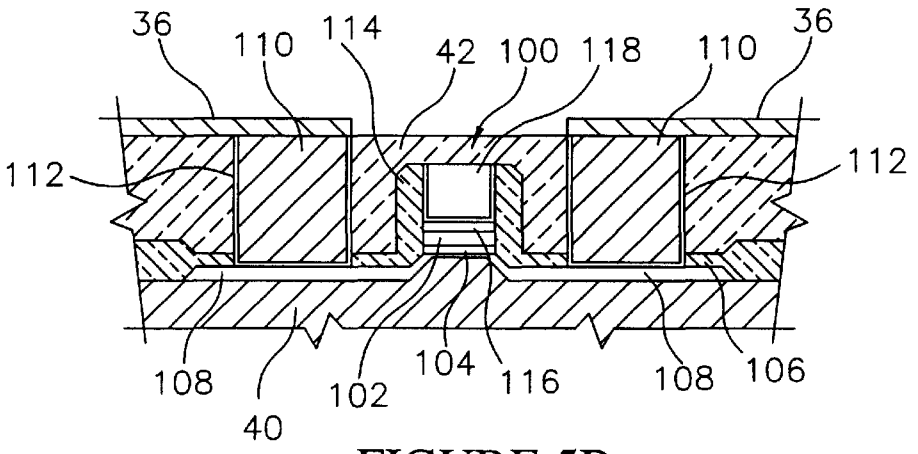


FIGURE 5B

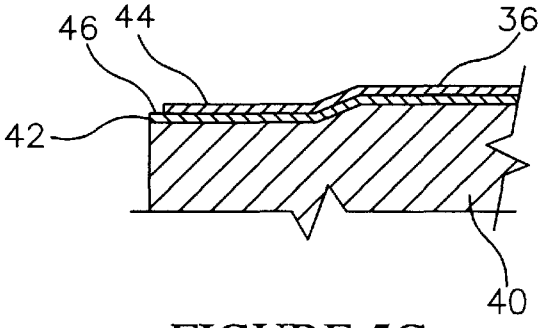


FIGURE 5C

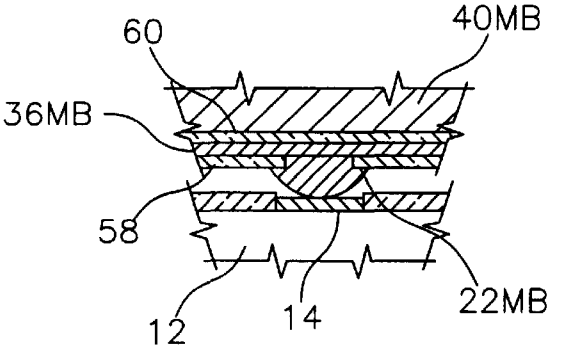


FIGURE 5D

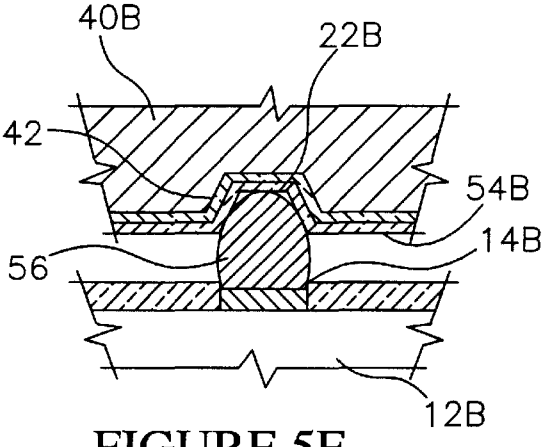


FIGURE 5E

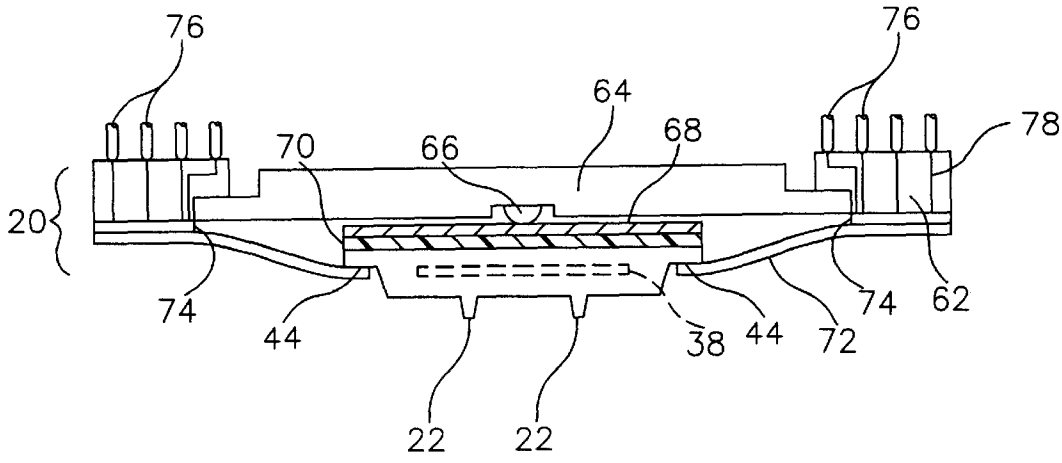


FIGURE 6

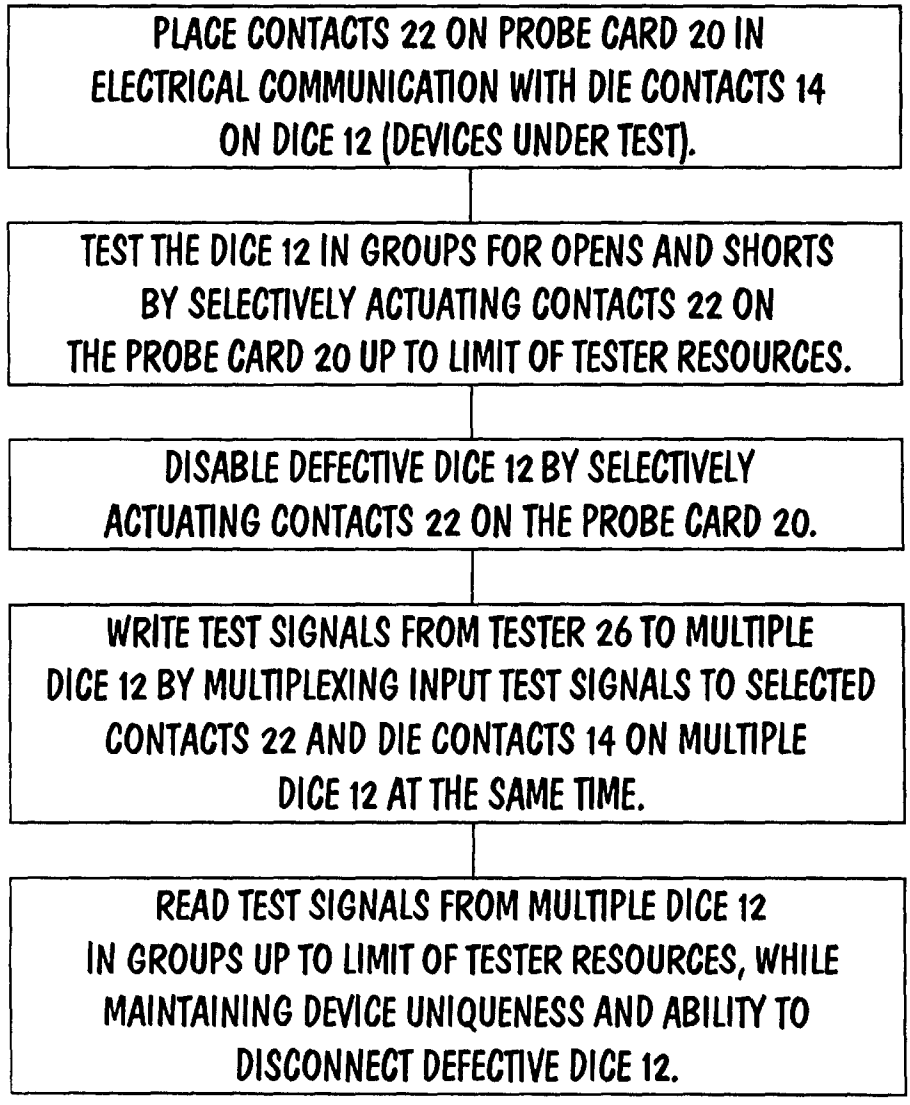


FIGURE 7

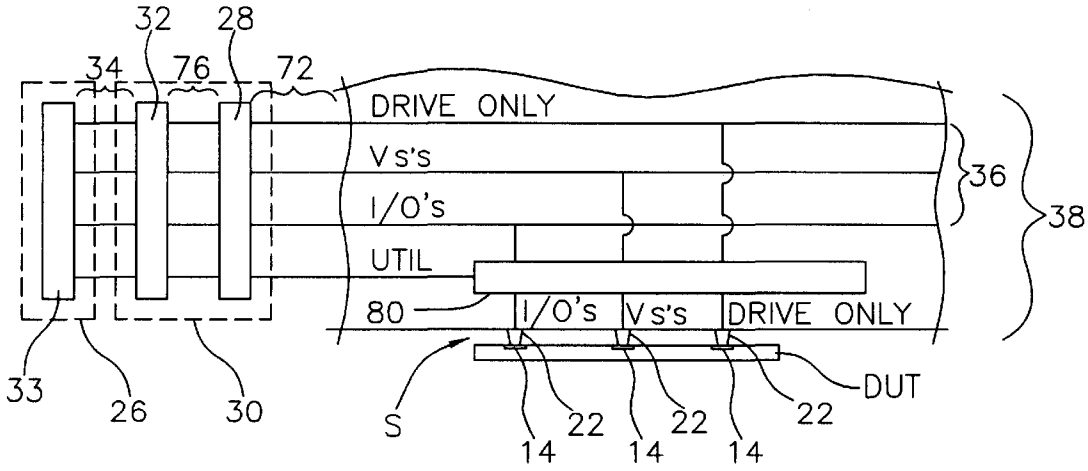


FIGURE 8A

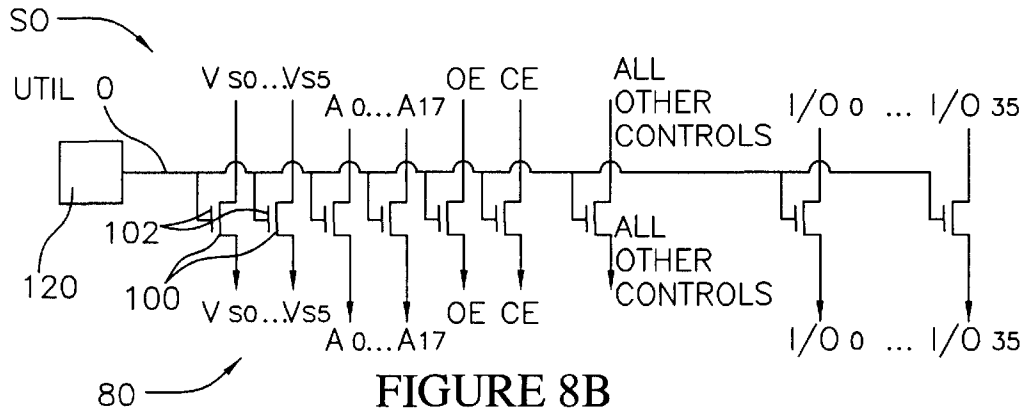


FIGURE 8B

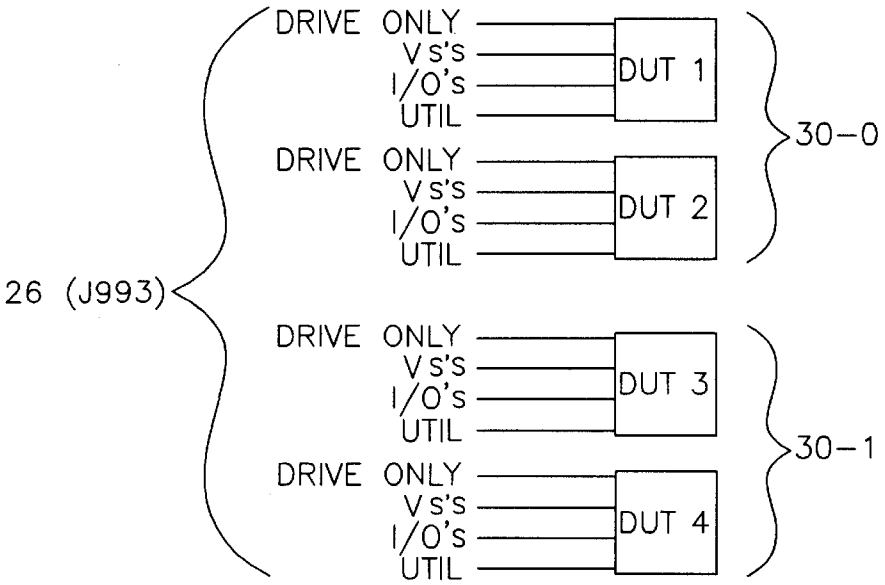
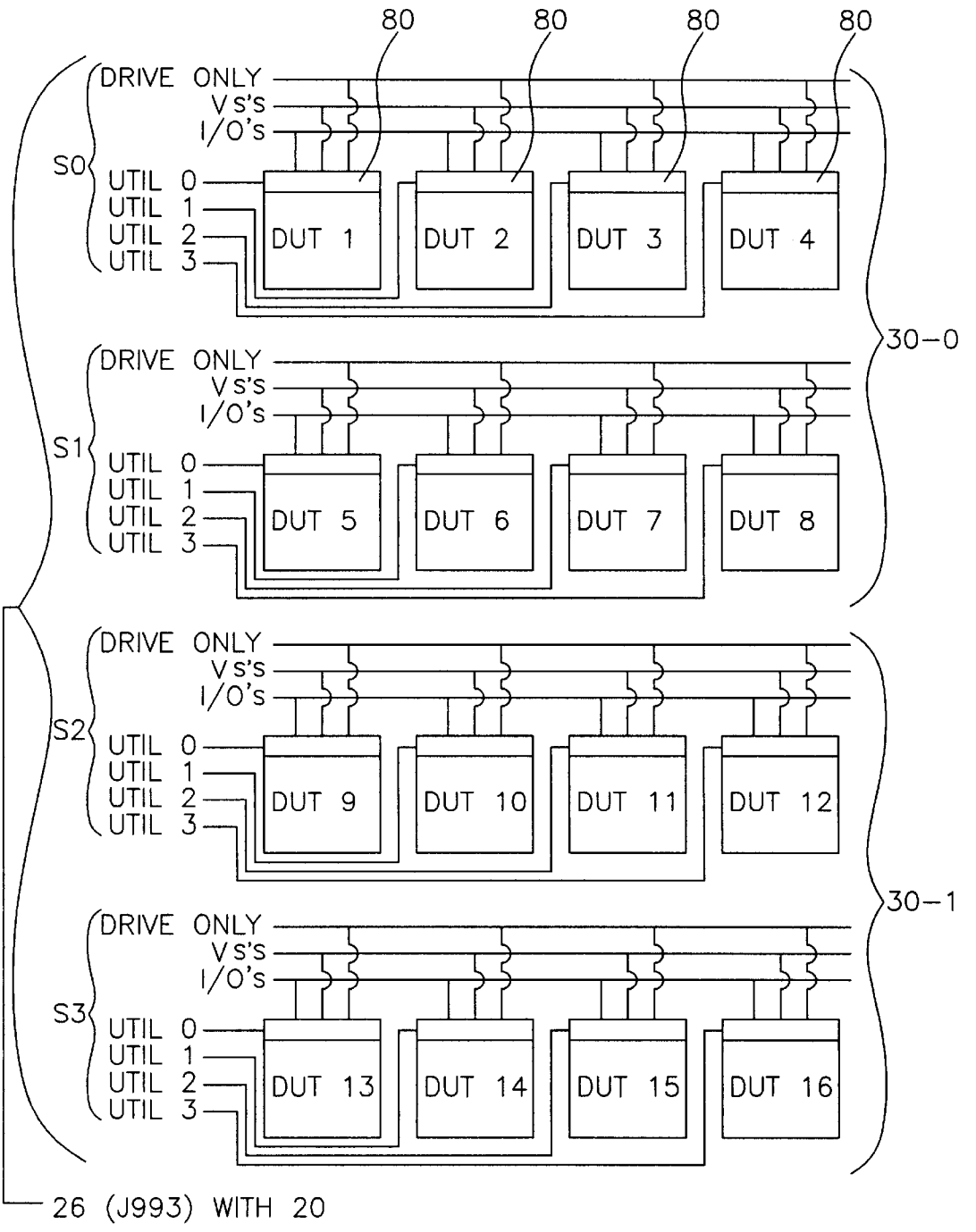


FIGURE 8C
(PRIOR ART)


80
80
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DRIVE ONLY
Vs's
I/O's
S0
UTIL 0
UTIL 1
UTIL 2
UTIL 3
DUT 1
DUT 2
DUT 3
DUT 4
30-0
S1
DUT 5
DUT 6
DUT 7
DUT 8
S2
DUT 9
DUT 10
DUT 11
DUT 12
30-1
S3
DUT 13
DUT 14
DUT 15
DUT 16
26 (J993) WITH 20

FIGURE 8D

PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of application Ser. No. 09/420,256, filed Oct. 18, 1999, U.S. Pat. No. 6,300,786 B1, which is a division of application Ser. No. 09/075,691 filed May 11, 1998, U.S. Pat. No. 6,246,250 B1.

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture and specifically to a probe card for testing semiconductor wafers. This invention also relates to test systems and test methods employing the probe card.

BACKGROUND OF THE INVENTION

Semiconductor wafers are tested prior to singulation into individual die, to assess the electrical characteristics of the integrated circuits contained on each die. A typical wafer-level test system includes a wafer prober for handling and positioning the wafers, a tester for generating test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board to route signals from the tester pin electronics to the probe card.

The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or mapped in software. Following testing, defective circuits can be repaired by actuating fuses to inactivate the defective circuitry and substitute redundant circuitry.

Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to electrically engage die contacts, such as bond pads, or other contacts on the wafer. An exemplary probe card having needle probes is described in U.S. Pat. No. 4,563,640 to Hasegawa et al.

Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, in which multiple dice must be tested at the same time. In addition, needle probe cards are not suitable for some applications in which the dice have high count die contact requirements, such as bond pads in dense grid arrays. In particular, the long needles and variations in the needles lengths makes it difficult to apply a constant gram force to each die contact. Long needles can also generate parasitic signals at high speeds (e.g., >500 MHZ).

A similar type of probe card includes buckle beams adapted to flex upon contact with the wafer. This type of probe card is described in U.S. Pat. No. 4,027,935 to Byrnes et al. Although better for high count die contacts, and high parallelism applications, buckle beam probe cards are expensive, and difficult to maintain.

Another type of probe card, referred to as a "membrane probe card", includes a membrane formed of a thin and flexible dielectric material such as polyimide. An exemplary membrane probe card is described in U.S. Pat. No. 4,918,383 to Huff et al. With membrane probe cards, contact bumps are formed on the membrane in electrical communication with conductive traces, typically formed of copper.

One disadvantage of membrane contact bumps is that large vertical "overdrive" forces are required to penetrate oxide layers and make a reliable electrical connection with the die contacts on the dice. These forces can damage the die contacts and the dice. In addition, membrane probe cards can be repeatedly stressed by the forces, causing the membrane to lose its resiliency. Use of high probe temperatures can also cause the membrane to lose resiliency.

Another disadvantage of membrane probe cards is the CTE (coefficient of thermal expansion) mismatch between the membrane probe card and wafer. In the future, with decreasing size of each die contact, higher parallelism requirements, and increased probing temperatures, maintaining electrical contact with the die contacts will be increasingly more difficult. In addition, because of relatively large differences between the CTE of membrane probe cards and silicon wafers, maintaining electrical contact between a large number of dice and a membrane probe card will be almost impossible.

Yet another limitation of conventional test systems, and a disadvantage of conventional probe cards, is that full functionality testing must be performed at the die level rather than at the wafer level. These tests require a large number of connections with the dice, and separate input/output paths between the dice and test circuitry. For functional test procedures on dice having multiple inputs and outputs, an input/output path must be provided to several die contacts at the same time. The number of dice that can be tested in parallel is always limited by the number of drive only, and input/output channels the tester provides, as well as the die contact arrangements on the dice. The number of drive only and input/output channels is fixed for a particular test system by its manufacturer.

To maintain speed characteristics for high count die contacts, the die contacts must be distributed throughout, or around the edges of the dice in a dense array. With this arrangement it is very difficult to parallel probe multiple dice using needle type probe cards, and impossible with dice having high count die contacts. Buckle beam probe cards are a costly alternative for probing dice having high count die contacts.

In view of the foregoing, improved probe cards capable of testing wafers with large numbers of dice, and high count die contacts, at high speeds, are needed in the art. In addition, probe cards capable of expanding tester resources to accommodate high parallelism, and high count die contact testing applications are needed in the art.

SUMMARY OF THE INVENTION

In accordance with the present invention, a probe card for testing semiconductor dice contained on a water is provided. The probe card is adapted for use with a conventional tester and wafer prober. The probe card includes an on board multiplex circuit adapted to fan out, and selectively transmit, test signals from the tester to the wafer in response to control signals. The multiplex circuit includes active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The multiplex circuit allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using the same tester resources.

In addition to the multiplex circuit, the probe card includes a substrate, and a pattern of contacts formed on the substrate. During a test procedure, the probe card contacts make temporary electrical connections with die contacts on the wafer. Each probe card contact can be enabled or disabled as required by the multiplex circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts.

The probe card and its contacts can be configured to electrically engage one die at a time, or multiple dice at the same time, up to all of the dice contained on the wafer. In an exemplary test procedure, dice can be tested for opens and shorts in groups corresponding to the available tester resources. Next, multiple dice can be written to in parallel by multiplexing drive only and I/O resources of the tester. Following the write step, multiple dice can be read in parallel in groups corresponding to the available tester drive only and I/O resources.

With the probe card comprising a semiconducting material such as silicon, the multiplex circuit can include integrated circuits and active electrical switching devices, formed directly on the substrate, using semiconductor circuit fabrication techniques. Alternately, the multiplex circuit can be fabricated on an interposer mounted to the probe card substrate, or on a die attached to the probe card substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a prior art semiconductor wafer containing multiple semiconductor dice;

FIG. **2** is a plan view of a prior art semiconductor die illustrating die contacts on a face of the die and exemplary functional designations for the die contacts;

FIG. **3** is a schematic cross sectional view of a test system constructed in accordance with the invention;

FIG. **4** is an enlarged plan view taken along section line **4**—**4** of FIG. **3** illustrating a probe card constructed in accordance with the invention;

FIG. **4**A is an enlarged plan view equivalent to FIG. **4** of an alternate embodiment probe card;

FIG. **4**B is a schematic cross sectional view of another alternate embodiment probe card;

FIG. **4**C is a schematic cross sectional view of another alternate embodiment probe card;

FIG. **5**A is an enlarged cross sectional view taken along section line **5**A—**5**A of FIG. **4**, following contact of the probe card and wafer, and illustrating probe card contacts electrically engaging die contacts on the wafer;

FIG. **5**B is an enlarged cross sectional view taken along section line **5**B—**5**B of FIG. **4**, illustrating a FET transistor of on board circuitry contained on the probe card;

FIG. **5**C is an enlarged cross sectional view taken along section line **5**C—**5**C of FIG. **4** illustrating a bonding pad on the probe card;

FIG. **5**D is an enlarged cross sectional view taken along section line **5**D—**5**D of FIG. **4**A illustrating an alternate embodiment probe card contact electrically engaging a die contact on the wafer;

FIG. **5**E is an enlarged cross sectional view taken along section line **5**E—**5**E of FIG. **4**A illustrating an alternate embodiment probe card contact electrically engaging a bumped die contact on the wafer;

FIG. **6** is an enlarged view of a portion of FIG. **3** illustrating the probe card;

FIG. **7** is a block diagram illustrating steps in a method for testing in accordance with the invention;

FIG. **8**A is a schematic electrical diagram of on board circuitry and a test site contained on the probe card and the electrical interface of the probe card and tester;

FIG. **8**B is a schematic electrical diagram of a multiplex circuit of the on board circuitry;

FIG. **8**C is a schematic electrical diagram illustrating a test operation for a tester with a prior art probe card; and

FIG. **8**D is a schematic electrical diagram illustrating a test operation for the tester of FIG. **8**C but with a probe card and multiplex circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1**, a prior art semiconductor wafer includes multiple semiconductor dice **12** fabricated using processes that are well known in the art. As shown in FIG. **2**, each die **12** includes multiple die contacts **14** formed thereon. The die contacts **14** comprise metal pads in electrical communication with integrated circuits contained on the die **12**.

Following singulation of the wafer **10**, the dice **12** can be packaged. In this case, the die contacts **14** can be wire bonded to lead fingers formed on a leadframe. The singulated dice **12** can also be used in unpackaged form as known good die (KGD). In this case, the die contacts **14** can be wire bonded to a substrate, such as a printed circuit board, or alternately flip chip mounted using reflowed solder bumps. The singulated dice **12** can also be included in chip scale packages. In this case, interconnects such as conductive bumps electrically contact the die contacts **14** to establish electrical communication with external contacts on a substrate.

For illustrative purposes, each die **12** includes twenty eight die contacts **14** with the functional designations indicated in FIG. **2**. However, as is apparent, the number and functional arrangements of the die contacts **14** are merely exemplary, and other arrangements are possible.

Referring to FIG. **3**, a test system **16** constructed in accordance with the invention, and configured to test the dice **12** contained on the wafer **10**. The test system **16** includes a test head **30** and a probe card **20**. The probe card **20** includes probe card contacts **22** configured to make temporary electrical connections with the die contacts **14**. The test system **16** also includes a wafer prober **18** wherein the probe card **20** is mounted, and a tester **26** configured to apply test signals through the probe card **20**, to the dice **12** contained on the wafer **10**, and to analyze the resultant signals. The wafer prober **18** includes a probe card holder **62** for mounting and electrically interfacing with the probe card **20**. Further details of the mounting of the probe card **20** to the test head **30** will be hereinafter described.

The wafer prober **18** includes a wafer chuck **24** configured to move in X and Y directions to align the wafer **10** with the probe card **20**, and in the Z direction to move the wafer **10** into contact with the probe card **20**. One suitable wafer prober **18** is manufactured by Electroglass and is designated a Model 4080.

The test system **16** also includes a prober interface board **28** for routing test signals from the test head **30** to the probe card **20**. In addition, the prober interface board **28** can be in electrical communication with tester pin electronics **32** in the test head **30**. The tester pin electronics **32** provide separate electrical paths **34** from test circuitry **33** contained in the tester **26**, to the test head **30** and to the prober interface board **28**.

The signal generating and analyzing capability of the test circuitry **33**, and the number of separate electrical paths **34** provided by the tester pin electronics **32**, are termed herein as "tester resources". In general, the configurations of the test circuitry **33**, and of the electrical paths **34**, are fixed for a particular tester **26** by the manufacturer. For example, the test circuitry **33** can be configured to route drive only signals through some of the electrical paths **34**, and input/output channels through other of the electrical paths **34**, as required for testing a particular type of die **12**. Exemplary testers **26** are commercially available from Teradyne of Boston Mass., as well as other manufacturers.

Referring to FIG. **4**, further details of the probe card **20** are illustrated. The contacts **22** on the probe card **20** are arranged in patterns corresponding to the patterns of the die contacts **14**. Each pattern of contacts **22** represents a single test site (S). For simplicity, only one pattern of contacts **22** and one test site (S) on the probe card **20** is illustrated. However, in actual practice, the probe card **20** can include multiple patterns of contacts **22** forming multiple test sites (S1 . . . Sn) to accommodate testing of multiple dice **12** at the same time. The contacts **22** on the test site S are designated **1–28** in correspondence with the die contacts **14** (FIG. **2**).

In order to test multiple dice **12** at the same time certain conditions must be met. Firstly, the patterns of contacts **22** must exactly match the patterns of the die contacts **14**. In addition, the stepping distance (i.e., x-y repeat and pattern spacing) must be the same for the contacts **22** as for the die contacts **14**. Secondly, the software that controls the stepping process must be able to pick valid test sites. For example, when testing at the edges of a round wafer with a probe card that includes rectangular or square patterns of contacts **22**, some patterns of contacts **22** will not have an associated device under test. It is also desirable to not have contacts **22** contacting a passivation layer **48** (FIG. **5A**) on the dice **12** as this can damage the contacts **22**.

In general, the use of the probe card **20** can greatly reduce the number of steps necessary for the prober **18** to test all of the dice **12** contained on the wafer **10**. In the extreme case, rather than using stepping methods, the probe card **20** can be formed with enough patterns of contacts **22** to simultaneously contact every die contact **14** for all of the dice **12** on the wafer **10**. Test signals can then be selectively applied and electronically switched as required, to selected dice **12** on the wafer **10**. The probe card **20** can be formed with any desired number of test sites (S1 . . . Sn). In addition, the probe card **20** can be configured to test a complete semiconductor wafer **10**, or to test a portion of the dice **12** in a partial wafer, or other substrate.

Still referring to FIG. **4**, in addition to the patterns of contacts **22**, the probe card **20** includes patterns of conductors **36** in electrical communication with the contacts **22** and with on-board circuitry **38**. The contacts **22** and conductors **36** are formed on a substrate **40** of the probe card **20**.

In the embodiment illustrated in FIG. **5A**, the substrate **40** comprises silicon (or another semiconducting material such as gallium arsenide). This permits the on-board circuitry **38** to be formed as integrated circuits on the substrate **40** using semiconductor circuit fabrication techniques such as doping, CVD, photolithography, and etching. Also, with the substrate **40** comprising silicon, a coefficient of thermal expansion of the probe card **20** exactly matches that of the wafer **10**. The substrate **40** can also comprise a silicon containing material, such as silicon-on-glass, and the on board circuitry can be formed on a layer of the substrate **40**.

Preferably, the substrate **40** is thick enough to resist deflection and buckling during test procedures using the probe card **20**. In addition, an electrically insulating layer **42**, such as SiO_2, polyimide, or BPSG can be formed on the substrate **40** to provide insulation for the contacts **22** and conductors **36** from the bulk of the substrate **40**.

The conductors **36** on the substrate **40** are in electrical communication with the probe card contacts **22**, and with the on board circuitry **38**. The conductors **36** can be formed on a surface of the substrate **40** in a required pattern. In addition, the conductors **36** can include interlevel segments, such as metal vias or other interlevel electrical paths, that are in electrical communication with other components of the on-board circuitry **38**.

In addition, the conductors **36** can be placed in electrical communication with the test circuitry **33** to provide electrical paths from the test circuitry **33** (FIG. **3**) to the on-board circuitry **38**, and to the contacts **22**. Preferably, the conductors **36** comprise a highly conductive metal such as copper, aluminum, titanium, tantalum, tungsten, molybdenum or alloys of these metals. The conductors **36** can be formed as a single layer of metal, or as a multi metal stack, using a thin film metallization process (e.g., CVD, patterning, etching). Alternately, a thick film metallization process (e.g., screen printing, stenciling) can be used to form the conductors **36**.

The conductors **36** also include bonding pads **44** located along the peripheral edges of the probe card **20**. The bonding pads **44** provide bonding sites for forming separate electrical paths from the probe card holder **62** (FIG. **1**) to each of the conductors **36**. Preferably the bonding pads **44** are located on recessed surfaces **46** (FIG. **5C**) along the edges of the substrate **40** to provide clearance for TAB bonds, wire bonds, spring loaded connectors (e.g., "POGO PINS") or other electrical connections to the bonding pads **44**.

Referring to FIG. **5A**, the probe card contacts **22** are shown in an enlarged cross sectional view. In the embodiment of FIG. **5A**, the contacts **22** comprise raised members that project from a surface of the substrate **40**. The raised contacts **22** help to provide a separation distance between the probe card **20** and the wafer **10** to clear any particulate contaminants that may be present on the opposing surfaces. In addition, the contacts **22** can include penetrating projections **50** adapted to penetrate the die contacts **14** to a limited penetration depth. To limit the penetration depth, the penetrating projections **50** have a height that is less than a thickness of the die contacts **14**. For thin film aluminum die contacts **14**, this thickness will typically be less than about 1.0 μm. As also shown in FIG. **5A**, surfaces **52** at the tips of the contacts **22** provide stop planes for limiting penetration of the contacts **22** into the die contacts **14**. These stop plane surfaces **52** along with the dimensions of the penetrating projections **50** insures that the contacts **22** minimally damage the die contacts **14** during a test procedure.

The contacts **22** and penetrating projections **50** can be formed integrally with the substrate **40** using a bulk micromachining process. With such a process, an etch mask (e.g., Si_3N_4 layer) can be formed on the substrate **40** and a suitable etchant, such as KOH, can be used to etch the substrate **40** to form the contacts **22**. Solid areas of the etch mask determine the peripheral dimensions and shape of the contacts **22**. The etch rate and time of the etch process determine the etch depth and the height of the contacts **22**. Such a process permits the contacts **22**, and penetrating projections **50**, to be formed accurately, and in a dense array to accommodate testing of dense arrays of die contacts **14**.

A representative height of the contacts **22** can be from 50 μm to 100 μm. A representative width of the contacts **22** on

a side can be from 25 μm to 80 μm. A spacing of the contacts **22** matches the spacing of the die contacts **14**. A height of the penetrating projections **50** can be from about 2000 Å–5000 Å.

Still referring to FIG. **5**A, each contact **22** is covered with a conductive layer **54** in electrical communication with a conductor **36**. The conductive layers **54** for all of the contacts **22** can be formed of a metal layer deposited and patterned to cover the contacts **22**, or other selected areas of the substrate **40**. By way of example, the conductive layers **54** for the contacts **22** can comprise aluminum, copper, titanium, tungsten, tantalum, platinum, molybdenum, cobalt, nickel, gold, iridium or alloys of these metals. Some of these materials such as gold and platinum are non-reactive so that material transfer between the contacts **22** and the die contacts **14** can be minimized. The conductive layers **54** can also comprise a metal silicide or a conductive material such as doped polysilicon. Further, the conductive layers **54** can comprise a bi-metal stack including a base layer, and a non-reactive and oxidation resistant outer layer, such as gold or platinum.

The conductive layers **54** can be formed using a metallization process that includes blanket deposition (e.g., CVD), formation of a resist mask, and then etching. Preferably, the resist mask comprises a thick film resist that can be deposited to a thickness greater than a conventional resist. One suitable resist is a negative tone, thick film resist sold by Shell Chemical under the trademark "EPON RESIN SU-8".

The conductive layer **54** for each contact **22** is in electrical communication with a corresponding conductor **36** formed on the substrate **40**. The conductive layers **54** and conductors **36** can be formed at the same time using the same metallization process. Alternately, the conductors **36** can be formed of a different metal than the conductive layers **54** using separate metallization process.

A process for fabricating the contacts **22** on a silicon substrate, substantially as shown in FIG. **5**A is described in U.S. Pat. No. 5,483,741, entitled "METHOD FOR FABRICATING A SELF LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE", and in U.S. Pat. No. 5,686,317 entitled "METHOD FOR FORMING AN INTERCONNECT HAVING A PENETRATION LIMITED CONTACT STRUCTURE FOR ESTABLISHING A TEMPORARY ELECTRICAL CONNECTION WITH A SEMICONDUCTOR DIE", both of which are incorporated herein by reference.

Referring to FIG. **5**B, an enlarged cross sectional view of a FET transistor **100** of the on board circuitry **38** is illustrated. As is apparent the FET transistor **100** is merely one component of the on board circuitry **38**. The on board circuitry **38** can include many FET transistors **100**, as well as additional components, to provide the circuit arrangements that will be hereinafter explained. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor **100** illustrated in the preferred embodiment.

The FET transistors **100** can be formed integrally with the substrate **40** using semiconductor circuit fabrication techniques. A suitable process sequence can include initially etching the contacts **22** (FIG. **5**A) and penetrating projections **50** (FIG. **5**A) and then fabricating the FET transistors **100**. Following formation of the FET transistors **100**, the insulating layer **42** can be formed, the conductive layers **54** (FIG. **5**A) can be formed, and the conductors **36** can be formed. Each FET transistor **100** includes a polysilicon gate **102**, and a gate oxide **104**. In addition, a field oxide **106** is formed on the substrate **40** for electrically isolating the FET transistors **100**. The substrate **40** also includes N+ active areas **108**, which can be formed by implanting dopants into the substrate **40** to form the sources and drains of the FET transistors **100**. Metal filled vias **110** with metal silicide layers **112**, electrically connect the sources and drains of the FET transistors **100** to the conductors **36**. The FET transistors **100** also include spacers **114**, TEOS layers **116** and nitride caps **118**.

Referring to FIG. **4**A, an alternate embodiment probe card **20**A is illustrated. The probe card **20**A is substantially similar to the probe card **20** previously described, but includes on board circuitry **38**A formed on a surface of the substrate **40** rather than being formed integrally therewith. For example, the on board circuitry **38**A can be included in a separate die mounted to the substrate **40**, and then interconnected to the conductors **36**. In this case the die containing the on board circuitry can be wire bonded or flip chip mounted to the substrate **40** in electrical communication with the contacts **14**. In this embodiment the substrate **40** can comprise silicon, ceramic, or a glass filled resin (FR-4).

As another alternative, the on board circuitry can be included on an interposer attached to the probe card **20**. Examples of interposers are shown in FIGS. **4**B and **4**C. In FIG. **4**B, an interposer **84**B includes on-board circuitry **38**B, substantially as previously described. The interposer **84**B can comprise a semiconducting material such as silicon, in which case the on-board circuitry **38**B can be fabricated on the interposer **84**B using semiconductor circuit fabrication techniques. Wire **88** can then be bonded to pads on the probe card **20** and to pads on the interposer **84**A to provide separate electrical paths there between.

Alternately, as shown in FIG. **4**C, on-board circuitry **38**C can be contained on a die **86** attached to an interposer **84**C (or directly to the probe card **20**). In the embodiment of FIG. **4**C, the die **86** is flip chip mounted to the interposer **84**C. Reflowed solder bumps **90** on the die **86** are bonded to internal conductors **92** on the interposer **84**C. In addition, the internal conductors **92** are in electrical communication with the contacts **22** on the probe card **20**.

Referring to FIG. **5**D, the probe card **20**A can include contacts **22**MB which are attached to the substrate **40** rather than being formed integrally therewith. As shown in FIG. **5**D, the probe card contacts **22**MB comprise metal microbumps formed on a polymer film **58** similar to multi layered TAB tape. In addition, conductors **36**MB are formed on an opposing side of the polymer film **58** in electrical communication with the contacts **22**MB. A compliant adhesive layer **60** attaches the polymer film **58** to a substrate **40**MB. Further details of contact **22**MB are described in U.S. Pat. No. 5,678,301, entitled "METHOD FOR FORMING AN INTERCONNECT FOR TESTING UNPACKAGED SEMICONDUCTOR DICE".

Another alternate embodiment probe card contact **22**B is illustrated in FIG. **5**E. Contacts **22**B are configured to electrically engage die contacts **14**B having solder bumps **56** formed thereon. The contacts **22**B permit a bumped die **12**B to be tested. The contacts **22**B comprise indentations formed in a substrate **40**B. In this embodiment the substrate can comprise silicon, gallium arsenide, ceramic or other substrate material. The indentations can be etched or machined to a required size and shape and then covered with conductive layers **54**B. The contacts **22**B are configured to retain the soder bumps **56**. In addition, the conductive layers **54**B for the contacts **22**B are in electrical communication with conductors equivalent to the conductors **36** previously

described. Further details of contact **22**B are described in U.S. patent application Ser. No. 08/829,193, now U.S. Pat. No. 5,962,921, entitled "INTERCONNECT HAVING RECESSED COBTACT MEMBERS WITH PENETRATING BLADES FOR TESTING SEMICONDUCTOR DICE AND PACKAGES WITH CONTACT BUMPS", incorporated herein by reference.

Referring to FIG. **6**, further details of the test system **16** and probe card **20** are illustrated. The wafer prober **18** includes the probe card holder **62**, a force applying fixture **64** and a force applying mechanism **66**. These items can be components of a conventional wafer prober as previously described. The force applying mechanism **66** presses against a pressure plate **68** and a compressible member **70** to bias the probe card **20** against the wafer **10**. By way of example, the compressible member **70** can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane **72** is bonded to the probe card **20** and to the probe card holder **62**. In general, the flexible membrane **72** functions to physically attach the probe card **20** to the probe card holder **62**. In addition, the flexible membrane **72** functions to provide electrical paths between the contacts **22** and the test circuitry **33** (FIG. **3**) of the tester **26**. The flexible membrane **72** can be formed of thin flexible materials to allow movement of the probe card **20** in Z-directions. For example, the flexible membrane **72** can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane **72** comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane **72** and corresponding conductors **74** on the probe card holder **62**. In addition, bonded connections are formed between the conductors on the membrane **72** and the bonding pads **44** on the probe card **20**.

Still referring to FIG. **6**, the wafer prober **18** includes spring loaded electrical connectors **76** which are in electrical communication with the prober interface board **28**. One type of spring loaded electrical connector **76** is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors **76** electrically communicate with internal conductors **78** on the probe card holder **62**.

The probe card mounting arrangement shown in FIG. **6**, as well as others, are described in U.S. patent application Ser. No. 08/797,719, entitled "PROBE CARD FOR SEMICONDUCTOR WAFERS AND METHOD AND SYSTEM FOR TESTING WAFERS", incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary and the probe card **20** can be mounted in a conventional manner on a commercially available wafer prober.

Test Method

Referring to FIG. **7**, steps in a method for testing the wafer **10** using the test system **18** and probe card **20** are illustrated. These steps are as follows.

1. Place contacts **22** on probe card **20** in electrical communication with die contacts **14** on dice **12** (devices under test).
2. Test the dice **12** in groups for opens and shorts by selectively actuating contacts **22** on the probe card **20** up to limit of tester resources.
3. Disable defective dice **12** by selectively actuating contacts **22** on the probe card **20**.
4. Write test signals from tester **26** to multiple dice **12** by multiplexing input test signals to selected contacts **22** and die contacts **14** on multiple dice **12** at the same time.
5. Read test signals from multiple dice **12** in groups up to limit of tester resources, while maintaining device uniqueness and ability to disconnect defective dice **12**.

Multiplex Circuit

Referring to FIGS. **8**A–**8**D, further details of the on board circuitry **38** (FIG. **4**A) are illustrated. In FIG. **8**A a single test site S is illustrated. The test site S on the probe card **20** includes a pattern of contacts **22** which are configured to electrically engage die contacts **14** on a device under test DUT. As previously described, the probe card **20** is in electrical communication with the probe card holder **62**, the tester pin electronics **32**, and the test circuitry **33** within the tester **26**.

As shown in FIG. **8**A, the on board circuitry **38** includes a multiplex circuit **80**. The multiplex circuit **80** is configured to receive test signals from the test circuitry **33** and to fan out or multiply the test signals. In addition, the multiplex circuit **80** is configured to selectively address the fanned out test signals through the probe card contacts **22** to selected die contacts **14** on the DUT. Stated differently, the multiplex circuit permits the test signals to be fanned out, allowing test procedures to be conducted in parallel. At the same time, the multiplex circuit **80** is configured to maintain the uniqueness of individual DUTs, and to electrically disconnect defective DUTs as required.

As shown in FIG. **8**A, the multiplex circuit **80** includes a Util channel for each DUT, which functions as a control channel. In addition to the Util channel, the multiplex circuit **80** includes drive only channels, Vs channels, and I/O channels. The numbers of the channels are determined by the tester resources. Table I lists the tester resources of a model "J993" tester **26** manufactured by Teradyne.

TABLE I

Tester Resources of Teradyne "J993" Tester
16 power supply channels per test head (30)
16X, 16Y address generation channels per test head (30)
16 DUTs can be tested in parallel per test head (30)
72 I/O channels per test head (30)
2 heads (30) per tester (26)
320 drive only channels per head (30) divisible as follows:
80 per test site (S) with 4 test sites (S0–S3)
40 per test site (S) with 8 test sites (S0–S7)
20 per test site (S) with 16 test sites (S0–S15)
Up to 320 megabits of catch RAM
36 Util channels per test head (30)

Table II lists the tester resources of a model "J994" tester **26** manufactured by Teradyne.

TABLE II

Tester Resources of Teradyne "J994" Tester
32 power supply channels per test head (30)
16X, 16Y address generation channels per test head (30)
32 DUTs can be tested in parallel per test head (30)
144 I/O channels per test head (30)
2 heads (30) per tester (26)
640 drive only channels per head 30 divisible as follows:
80 per test site (S) with 8 test sites (S1–S8)
40 per test site (S) with 16 test sites (S1–S16)
20 per test site (S) with 32 test sites (S1–S32)
Up to 640 megabits of catch RAM
52 Util channels per test head (30)

Table III lists the test requirements for one type of SRAM.

TABLE III

Sample SRAM Requirements For Each Device Under Test DUT
36 I/O channels per DUT
18 address channels (drive only) per DUT
32 control channels (drive only) per DUT
6 power supply channels (Vs-voltage supplies) per DUT
Util channels used depends on parallelism
Total
36 I/O channels per DUT
50 drive only channels per DUT
6 Vs channels per DUT

With these sample requirements a "J993" tester **26** can test two DUTs per test head **30**, due to the I/O requirements. This is shown schematically in FIG. **8**C. In FIG. **8**C, the (J993) tester **26** includes a first test head **30-0** and a second test head **30-1**. Each test head **30-0**, **30-1**, is capable of testing two DUTs, for a total of four at a time. Following testing of these four DUTs, both wafers **10** (one on each test head) can be stepped such that four additional DUTs align with the probe card contacts for testing.

A "J994" tester **26** has twice the tester resources of a "J993" tester **26**. Accordingly on the basis of the above sample I/O requirements, a "J994" tester **26** can test four DUTs per test head **30**, for a total of eight at a time.

Referring to FIG. **8**B, a single test site S of the multiplex circuit **80** is illustrated. The multiplex circuit **80**, simply stated, comprises multiple FET transistors **100** configured to provide a switching circuit for selectively enabling and disabling the contacts **22** on the probe card **20**. The gate **102** of each FET transistor **100** is in electrical communication with the Util **0** channel. A controller **120** (or computer) generates control signals which are transmitted through the Util **0** channel to the FET transistors **100**.

In the illustrative embodiment the multiplex circuit **80** is configured to test the SRAM of Table III. Accordingly, there are six Vs channels (Vs**0** . . . Vs**5**), eighteen address channels (A**0** . . . A**17**), and thirty six I/O channels (I/O**0**–I/O**35**). In addition, there is an OE channel, a CE channel, and an "all other controls" channel. With this arrangement test signals can be transmitted from the test circuitry **33** and latched by the channels. Control signals from the controller **120** then control the FET transistors **100** to enable and disable the contacts **22** to selectively transmit the test signals to the die contacts **14** as required.

During the test mode the uniqueness of each DUT is maintained. In addition, the control signals can be used operate the FET transistors **100** to disable selected contacts **22** in order to electrically disconnect defective DUTs. Still further, the control signals can be used to operate the FET transistors **100** to enable and disable selected contacts **22** in the transmission of "read" signals from the DUTs. However, in the "read" mode the DUTs must be read in accordance with the tester resources.

As is apparent, the multiplex circuit **80** illustrated in FIG. **8**B is merely exemplary. Those skilled in the art, with the aid of the present specification, can design other multiplex circuits able to multiply and selectively address test signals from a tester. Thus other types of multiplexing circuits are intended to be included within the scope of the present claims.

Referring to FIG. **8**D, the operation of the J993 tester **26** of Table I, outfitted with the probe card **20** having the multiplex circuit **80** is illustrated. In this example there are four test sites **S0**, **S1**, **S2**, **S4** contained in two test heads **30-0**, **30-1**. Using the multiplex circuit each test site can write test signals to four DUTs at a time. In the "read" mode the additional three DUTs per test site must be selected in accordance with tester resources (e.g., one at a time or two at a time).

A limiting factor in the number of DUTs that can be tested by each test site is the drive current capacity of the channels of the tester **26**. On the J993 and J994 testers **26**, the drive current capacity is about 50 mA per channel. In addition, the test signals can be specified with a current (IOL) of about 8 mA per channel. Thus with some margin, each I/O channel and drive only channel of the tester **26** can be configured to drive four DUTs substantially as shown in FIG. **8**D. During a write operation there is 8 mA per DUT X 4 DUTs=32 mA per tester drive only channel. This leaves a 18 mA per channel margin.

Thus the invention provides an improved probe card for testing semiconductors wafers, a method for testing semiconductor wafers using the probe card, and a test system employing the probe card. The probe card can include contacts in dense arrays to accommodate testing of multiple dice having dense arrays of die contacts. In addition, the probe card includes on board circuitry configured to expand tester resources.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts, the probe card contacts arranged in sets configured to electrically engage selected dice on the wafer;

an interposer on the substrate; and

a multiplex circuit on the interposer in electrical communication with the probe card contacts, the multiplex circuit configured to fan out test signals from a tester, and to control the probe card contacts to selectively transmit the test signals to the die contacts while the sets maintain a uniqueness of each die and disconnect defective dice.

2. The probe card of claim **1** wherein the interposer comprises a semiconductor die containing the multiplex circuit.

3. The probe card of claim **1** wherein the interposer is flip chip mounted or wire bonded to the substrate.

4. A probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts, the probe card contacts arranged in sets configured to electrically engage selected dice on the wafer;

a semiconductor die on the substrate; and

a multiplex circuit on the die in electrical communication with the probe card contacts, the multiplex circuit configured to fan out test signals from a tester, and to control the probe card contacts to selectively transmit the test signals to the die contacts, while the sets maintain a uniqueness of each die and disconnect defective dice.

5. The probe card of claim 4 wherein the die is wire bonded or flip chip mounted to the substrate.

6. The probe card of claim 4 wherein the die is mounted to an interposer attached to the substrate.

7. The probe card of claim 4 wherein the probe card contacts comprise raised members at least partially covered with conductive layers.

8. The probe card of claim 4 wherein the probe card comprises silicon and the probe card contacts comprise etched members having projections configured to penetrate the die contacts.

9. The probe card of claim 4 wherein the probe card contacts comprise microbumps on a polymer film attached to the probe card.

10. The probe card of claim 4 wherein the die contacts comprise bumps, and the probe card contacts comprise indentations configured to retain and electrically engage the bumps.

11. In a test system including a tester configured to generate test signals and having a signal writing capability, a probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts; and

a multiplex circuit on the substrate in electrical communication with the probe card contacts, the multiplex circuit configured to control the test signals to expand the signal writing capability of the tester, and to speed up the testing by multiplexing write test signals from the tester to the die contacts, by reading read test signals from selected groups of dice up to the signal reading capability, and by controlling the probe card contacts to disable defective dice.

12. The probe card of claim 11 wherein the multiplex circuit is contained on a die wire bonded or flip chip mounted to the substrate.

13. The probe card of claim 11 wherein the multiplex circuit is contained on a die mounted to an interposer attached to the substrate.

14. The probe card of claim 11 wherein the multiplex circuit is contained on an interposer attached to the substrate.

15. In a test system for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts, the system including a tester configured to generate and analyze test signals and having tester resources determined by a signal generating, transmitting and analyzing capability thereof, a probe card for applying the test signals to the dice comprising:

a substrate comprising a plurality of probe card contacts in electrical communication with the tester and configured to make temporary electrical connections with the die contacts;

a semiconductor die on the substrate; and

a multiplex circuit on the die in electrical communication with the probe card contacts, the multiplex circuit configured to control the test signals to speed up the testing, by fanning out the write test signals to multiple dice, and by reading the read test signals in groups up to a limit of the tester resources.

16. The probe card of claim 15 wherein the die is flip chip mounted or wire bonded to the substrate.

17. The probe card of claim 15 wherein the die is mounted to an interposer attached to the substrate.

18. The probe card of claim 15 wherein the multiplex circuit is contained on an interposer attached to the substrate.

19. The probe card of claim 15 wherein the probe card contacts comprise raised members at least partially covered with conductive layers.

20. The probe card of claim 15 wherein the probe card contacts comprise microbumps on a polymer film attached to the probe card.

21. The probe card of claim 15 wherein the die contacts comprise bumps, and the probe card contacts comprise indentations configured to electrically engage the bumps.

* * * * *

EXHIBIT J

US006798225B2

(12) **United States Patent**
Miller

(10) **Patent No.: US 6,798,225 B2**
(45) **Date of Patent: Sep. 28, 2004**

(54) **TESTER CHANNEL TO MULTIPLE IC TERMINALS**

(75) Inventor: **Charles A. Miller**, Fremont, CA (US)

(73) Assignee: **FormFactor, Inc.**, Livermore, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/142,550**

(22) Filed: **May 8, 2002**

(65) **Prior Publication Data**

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(52) **U.S. Cl.** **324/754**; 324/765

(58) **Field of Search** 324/754, 757–758, 324/760, 762, 765, 158.1; 714/724, 734, 738, 742; 333/33, 246–247; 702/85–89, 104–119

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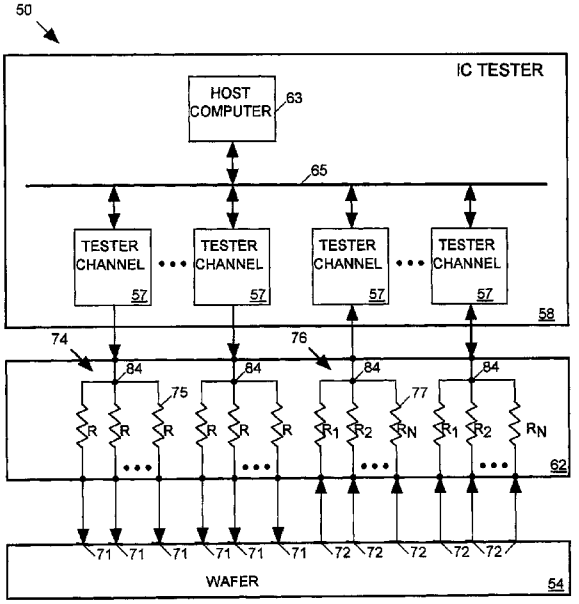
Assistant Examiner—Jermele Hollington
(74) *Attorney, Agent, or Firm*—Smith-Hill and Bedell

(57) **ABSTRACT**

A probe card provides signal paths between integrated circuit (IC) tester channels and probes accessing input and output pads of ICs to be tested. When a single tester channel is to access multiple (N) IC pads, the probe card provides a branching path linking the channel to each of the N IC input pads. Each branch of the test signal distribution path includes a resistor for isolating the IC input pad accessed via that branch from all other branches of the path so that a fault on that IC pad does not substantially affect the voltage of signals appearing on any other IC pad. When a single tester channel is to monitor output signals produced at N IC pads, the resistance in each branch of the signal path linking the pads of the tester channel is uniquely sized to that the voltage of the input signal supplied to the tester channel is a function of the combination of logic states of the signals produced at the N IC pads. The tester channel measures the voltage of its input signal so that the logic state of the signals produced at each of the N IC output pads can be determined from the measured voltage.

21 Claims, 6 Drawing Sheets



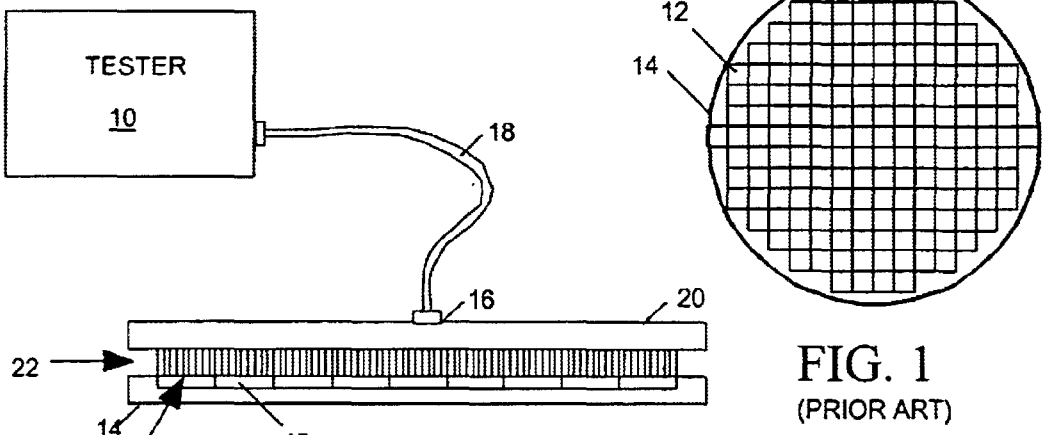


FIG. 1
(PRIOR ART)

FIG. 2
(PRIOR ART)

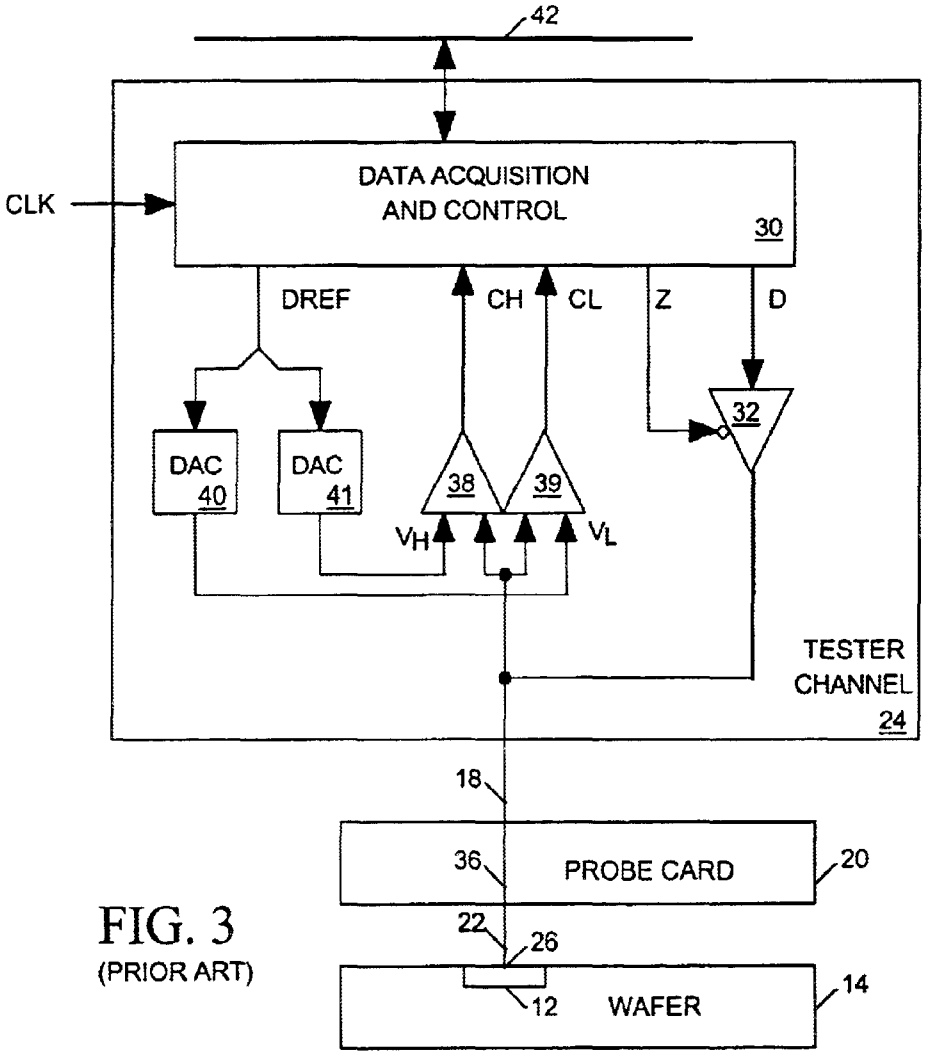
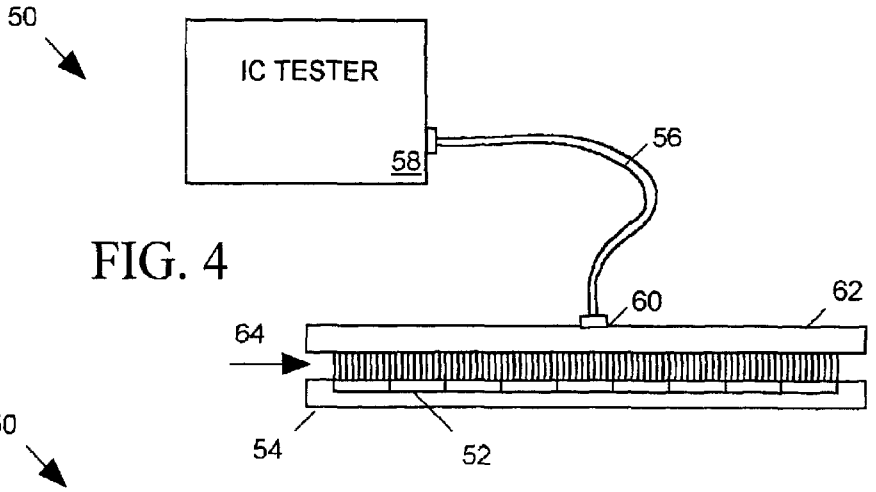


FIG. 3
(PRIOR ART)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IC TESTER
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56
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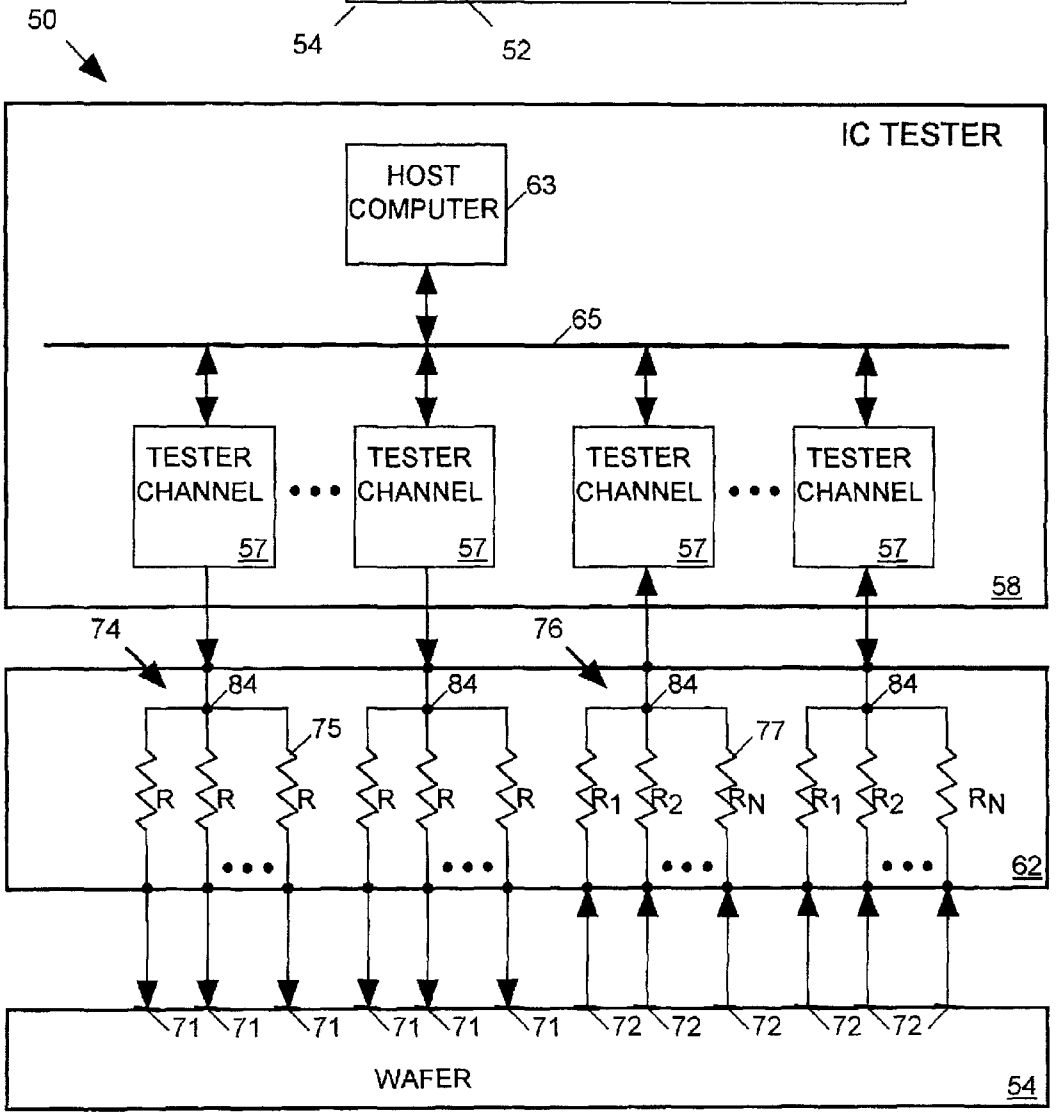
54
52

FIG. 4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IC TESTER
HOST COMPUTER
63
65
TESTER CHANNEL
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84
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R1
R2
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71
72
WAFER
54

FIG. 5

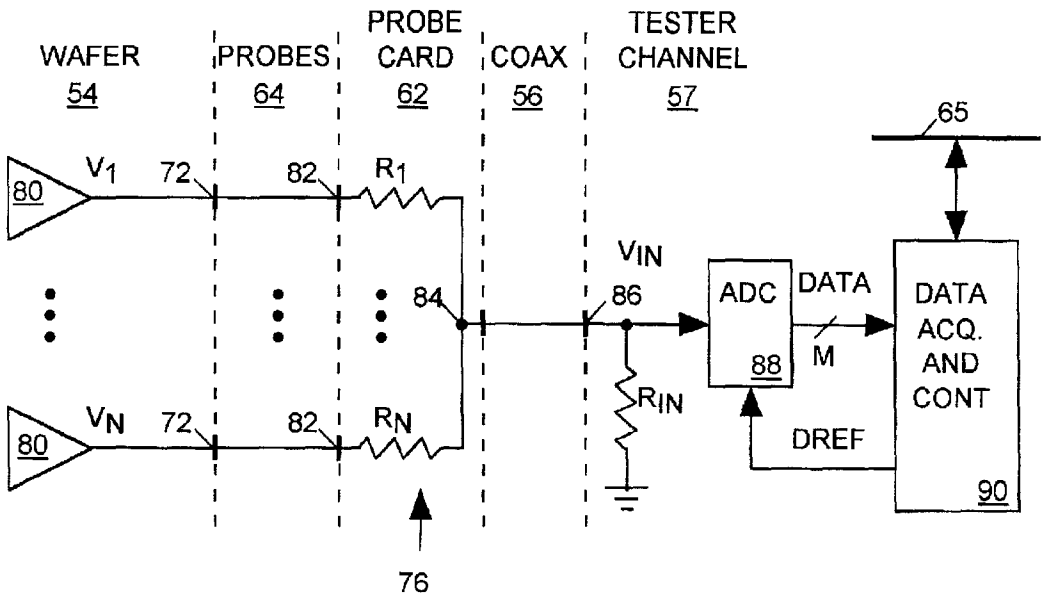

FIG. 6

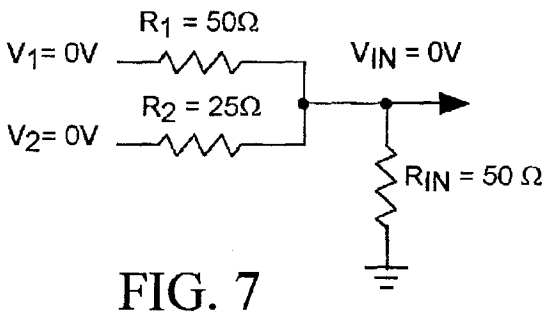

FIG. 7

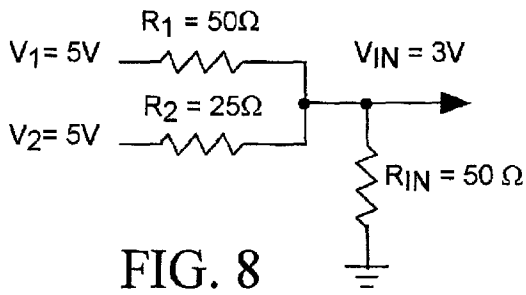

FIG. 8

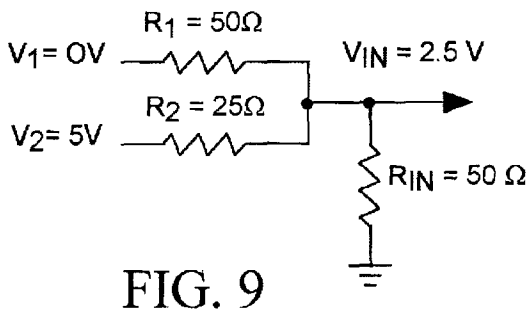

FIG. 9

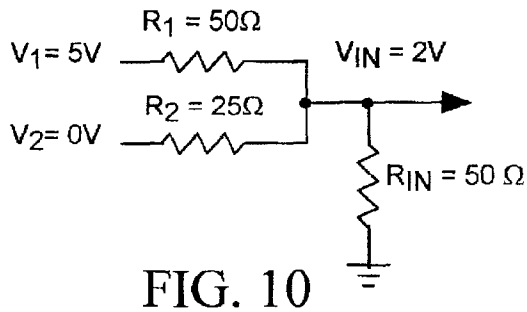

FIG. 10

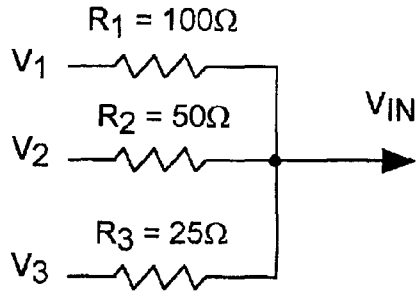
R1 = 100Ω
V1
R2 = 50Ω
V2
VIN
R3 = 25Ω
V3

FIG. 11

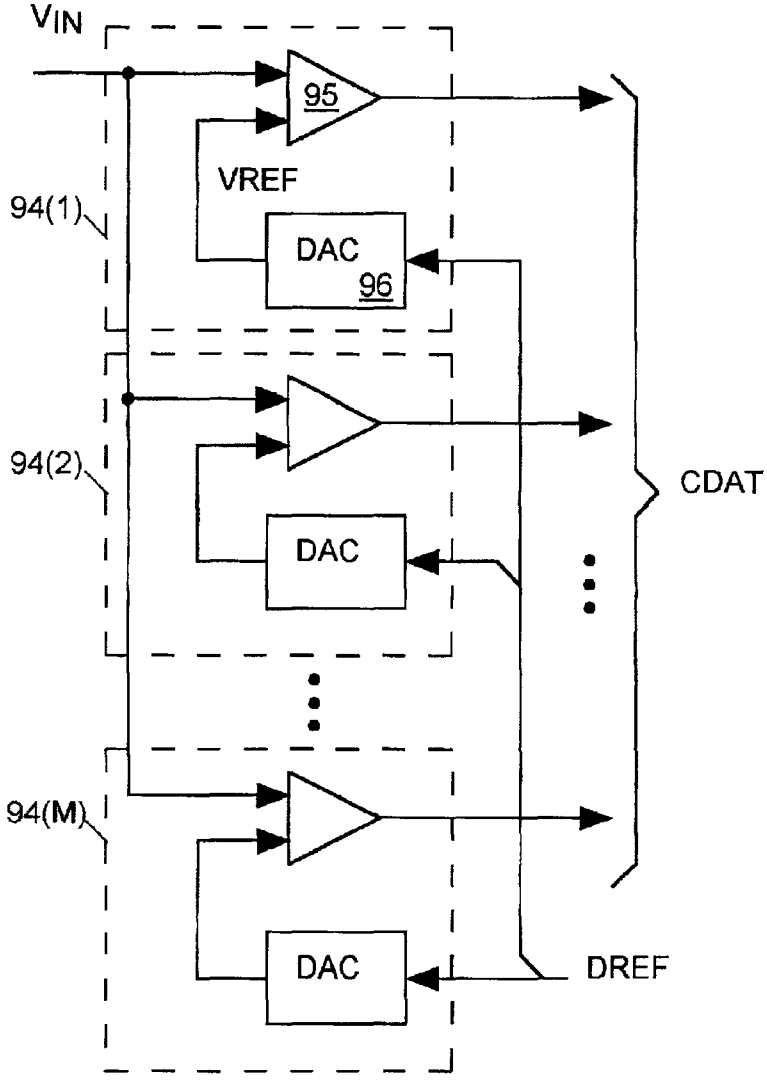
VIN
95
VREF
94(1)
DAC
96
94(2)
DAC
CDAT
94(M)
DAC
DREF

FIG. 12

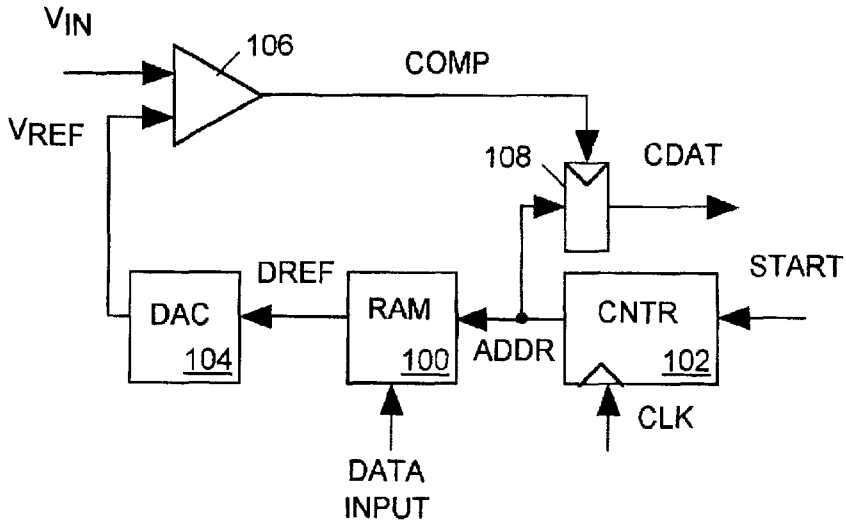
VIN
106
COMP
VREF
108
CDAT
START
DREF
DAC
104
RAM
100
ADDR
CNTR
102
CLK
DATA
INPUT

FIG. 13

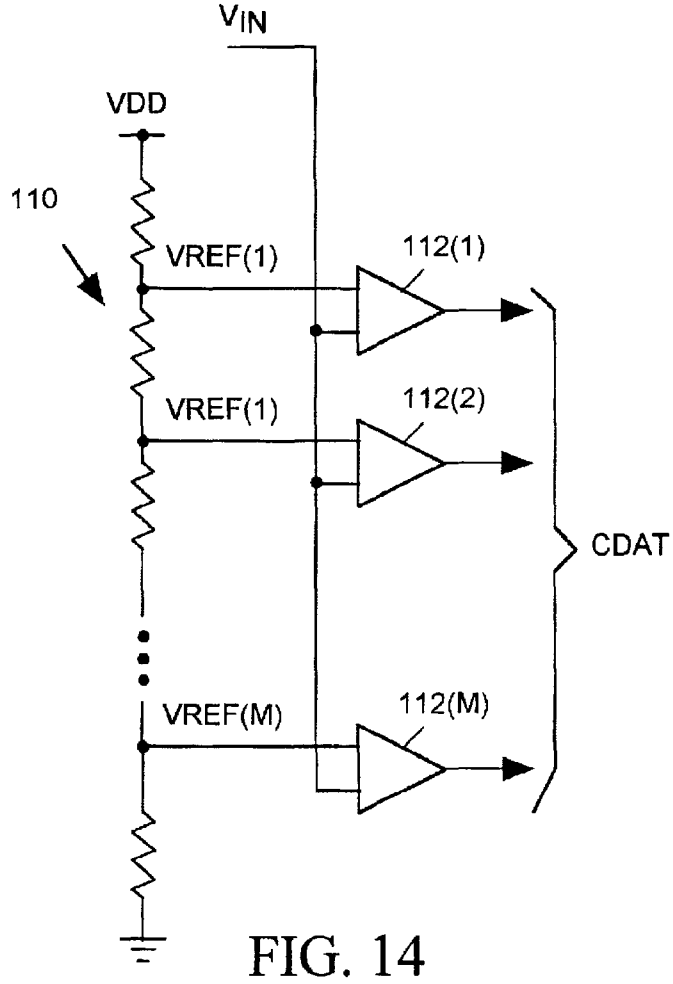
VIN
VDD
110
VREF(1)
112(1)
VREF(1)
112(2)
CDAT
VREF(M)
112(M)

FIG. 14

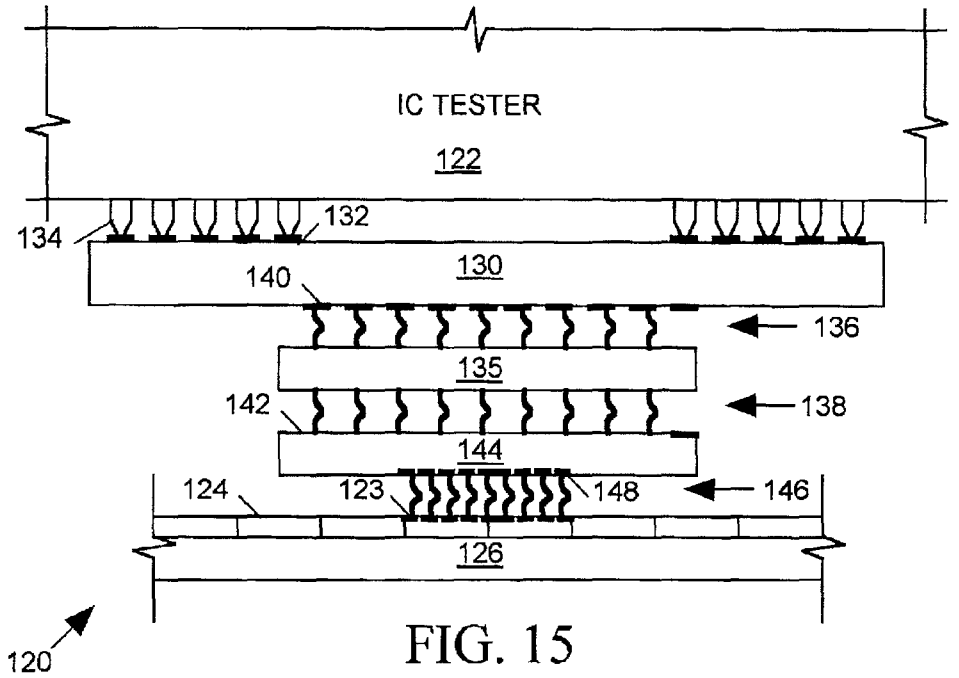

FIG. 15

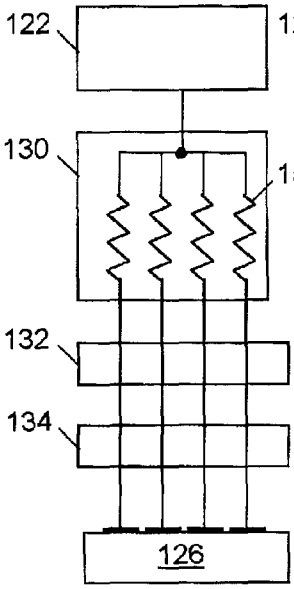

FIG. 16

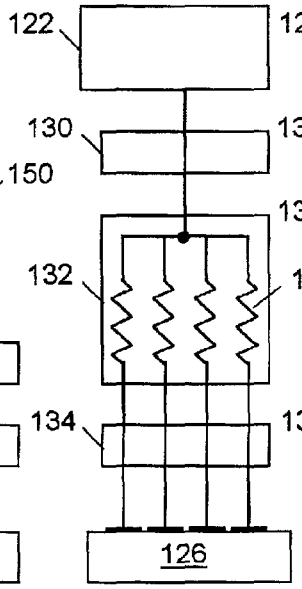

FIG. 17

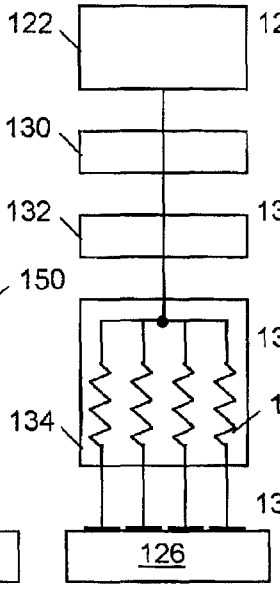

FIG. 18

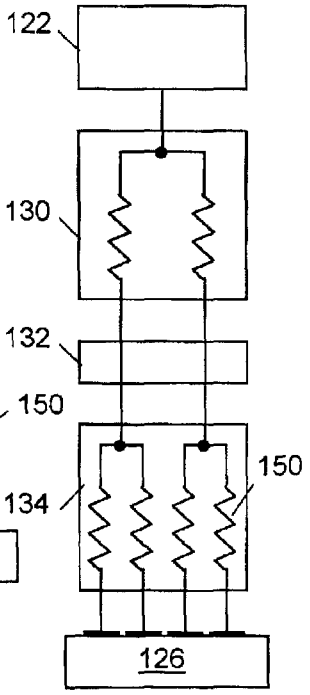

FIG. 19

TESTER CHANNEL TO MULTIPLE IC TERMINALS

FIELD OF THE INVENTION

The invention relates in general to systems for testing integrated circuits (ICs), and in particular to a system for distributing a single test signal output of an IC tester to multiple input terminals of one or more ICs and for determining states of output signals produced at multiple IC output terminals.

DESCRIPTION OF RELATED ART

As illustrated in FIG. **1**, an integrated circuit (IC) manufacturer fabricates an array of ICs **12** on a semiconductor wafer **14** and then cuts the wafer to separate the ICs from one another. The manufacturer may then install the ICs in separate packages using bond wires to link the IC's input/output (I/O) terminals (conductive pads on the surface of each IC) to package pins providing signal paths to external circuits. Some ICs include "redistribution" layers covering its I/O terminals. Conductors within the redistribution layers link the IC's I/O terminals to contact pads formed on the top surface of the redistribution layers. The contact pads are larger than the IC's I/O terminals and are more evenly distributed so that the IC can be mounted directly on printed circuit boards (PCBs), for example by soldering the pads to correspondingly arranged contact pads on the surfaces of the PCBs. Spring contacts can also be used to link the IC's redistributed contact pads to a PCB's contact pads. The spring contacts may be formed either on the IC's contact pads or on the PCB's contact pads.

ICs may be tested at the wafer level before they are separated from one another or may be tested after they have separated. Referring to FIG. **2**, an IC tester **10** for testing an array of ICs **12** residing on a wafer **14** (or for testing an array of singulated ICs held on a tray) typically includes a set of tester channels, each of which may either transmit a test signal to an IC input pad or monitor an IC output signal produced at an IC output pad to determine whether the IC responds correctly to its input signals. A set of coaxial cables **18** provides signal paths between the tester channels and a cable connector **16** on a probe board **20**. A set of probes **22** link pads on the lower surface of probe board **20** to the redistribution or I/O terminal pads on the upper surfaces of ICs **12**. Various types of structures can be used to implement probes **22** including, for example, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are used to implement probes **22** they may be formed either on pads on the upper surfaces of ICs **12** or on pads on the lower surface of probe board **20**.

U.S. Pat. No. 6,064,213, issued May 16, 2000 to Khandros et al., incorporated herein by reference, discloses an example of a card assembly designed to contact spring contacts formed on an IC. U.S. patent application Ser. No. 09/810,871 filed Mar. 16, 2001 (incorporated herein by reference) describes another example of a card assembly employing spring contact probes. U.S. Pat. No. 5,974,662 issued Nov. 2, 1999, issued to Eldridge et al., incorporated herein by reference, descries an example of a probe card assembly in which spring contacts formed on a probe card function as probes. The following documents (incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No. 6,333,269 issued Jan. 8, 2002 to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Probe board **20** is typically a multiple layer printed circuit board (PCB) providing signal paths between cable connector **16** and the pads on its lower surface. Traces formed on the various layers of probe board **20** convey signals horizontally while vias convey signals vertically though the layers.

Tester **10** typically provides a separate channel for each pad **26** that is linked to an I/O terminal of an IC to be tested. FIG. **3** illustrates one channel **24** of a typical tester accessing a pad **26** of a wafer **14** via a path **36** through a probe card **20**. A test is usually organized into a succession of test cycles of uniform duration, and during each test cycle channel **24** may either provide an input to a pad **26** of an IC **12** formed on wafer **14** or may monitor an IC output signal produced by the IC at pad **26** to determine its state. A data acquisition and control circuit **30**, programmed via instructions supplied through a bus **42**, controls the action channel **24** is to carry out during each test cycle. When pad **26** is to receive an input signal, circuit **30** sets a tristate control input Z of a tristate driver **32** so that the driver supplies a test signal as input to pad **26**. Circuit **30** sets an input signal D to driver **32** during each test cycle so that the test signal is of the correct logic state. The test signal travels to pad **26** through a signal path formed by one of cables **18**, the signal path **36** provided by probe card **20**, and one of probes **22**.

When an IC **12** produces an output signal at pad **26**, the output signal passes through probe **22**, signal path **36** and cable **18** to become an input signal to a pair of comparators **38** and **39** within channel **24**. Comparator **38** asserts a compare high (CH) signal when the voltage of IC output signal is higher than a high logic level threshold voltage produced by a digital-to-analog converter (DAC) **40**. Comparator **39** asserts a compare low (CL) signal when the IC output signal voltage is lower than a low logic level threshold voltage produced by another digital-to-analog converter (DAC) **41**. Circuit **30** supplies control data DREF as input to DACs **40** and **41** for controlling the voltage levels of the VH and VL reference signals.

For example, when the test signal has 5 volt and 0 volt high and low logic levels, the VH and VL threshold levels might be set to 4.5 and 0.5 volts, respectively, so that an IC output signal over 4.5 volts is treated as a high logic level, an IC output signal under 0.5 volts is treated as a low logic level, and an IC output signal between 0.5 and 4.5 volts is considered neither high nor low logic level. Thus comparators **38** and **39** and DACs **40** and **41** can be thought of as an analog-to-digital converter (ADC) producing a 2-bit thermometer code output {CH, CL} indicating one of three ranges in which the input signal voltage lies.

Data acquisition circuit **30** samples the CH and CL bits at a time during each test cycle when the IC output signal is expected to be at a particular logic level. If the IC output signal is expected to be at its high logic level, then the CH bit should be true and the CL bit should be false when sampled. If the IC output signal is expected to be at is low logic level then CL should be true and CH should be false when sampled. An IC under test is considered to be defective when the sampled CH and CL bits representing the state of any of the IC's output signals are not of their expected states during any test cycle.

In some testers data acquisition and control circuit **30** stores the CH and CL bit for each test cycle in an acquisition memory so that a host computer can access the data via bus **42** at the end of the test and determine whether the IC is defective. In other testers circuit **30** may compare the

sampled CH and CL data produced during each test cycle to their expected values and store cycle numbers in an internal memory referencing the particular test cycles, if any, for which the sampled data fails to match their expected values. The host computer then accesses the stored cycle numbers via bus **42**.

While tester channels **24** in some testers include two comparators as illustrated in FIG. **3**, tester channels in other testers may include only a single comparator. For example when the low and high logic levels of an IC output signal are 0 and 5 volts, respectively, the comparator may be set to drive its single-bit output signal true when the IC output signal exceeds 2.5 volts. Also in many testers channel do not include their own DACs; centralized DACs provide reference voltages in common to all channels.

One drawback to the test system illustrated in FIGS. **2** and **3** is that it requires one tester channel **24** for every pad **26** on wafer **14**. Since a wafer **14** can have a large number of ICs **12**, and since each IC may have a large number of such pads **26**, tester **10** would require a very large number of channels in order to concurrently access all pads **26** of all ICs **12**.

What is needed is a system permitting a tester having a limited number of tester channels to concurrently test ICs having a larger number of input and output pads.

BRIEF SUMMARY OF THE INVENTION

Integrated circuits (ICs) formed on a semiconductor typically include conductive pads on their surfaces for receiving IC input signals and for transmitting IC output signals. The invention relates in general to a system for testing ICs before the wafer is cut to separate them, and in particular to an interconnect system for linking a single IC tester channel to multiple (N) IC input or output pads in a way that allows the tester channel to either concurrently transmit a test signal to all N IC input pads or to concurrently monitor and determine states of output signals produced at all N IC output pads.

An interconnect system in accordance with an exemplary embodiment of the invention may include a probe card providing signal paths between the various channels of an IC tester and probes accessing the input and output pads on the surface of the ICs. When a single tester channel is to be connected to each of N IC pads, the probe card provides a branching signal path for distributing the test signal produced by the tester channel to probes accessing each of the N IC pads. Each branch of the path includes a resistor for isolating the IC input pad accessed via that branch from all other branches of the path so that a fault on the IC input pad accessed via that branch does not substantially affect the voltage of the test signal passing through any other branch.

When a single tester channel is to transmit a test signal to all N IC pads, but is not to monitor IC output signals produced at any N IC pads, the resistance of the resistors included in all path branches may be of similar size. However when a single tester channel is to monitor IC output signals produced at all N IC pads, each branch includes a uniquely sized scaling resistor so that each of the 2^N combinations of logic states of the signals produced at the N IC output pads results in a different tester channel input signal voltage. In such case, the tester channel measures the voltage of its input signal and the logic state of each of the signals produced at each of the N IC output pads is determined from the measured voltage of the input signal.

The claims appended to this specification particularly point out and distinctly claim the subject matter of the invention. However those skilled in the art will best understand both the organization and method of operation of what the applicant considers to be the best modes of practicing the invention, together with further advantages and objects of the invention, by reading the remaining portions of the specification in view of the accompanying drawings wherein like reference characters refer to like elements.

BRIEF DESCRIPTION OF THE DRAWING(S)

FIG. **1** is a plan view of a prior art semiconductor wafer upon which integrated circuits (ICs) are formed,

FIG. **2** is a simplified side elevation view of a prior art wafer level IC test system,

FIG. **3** is a block diagram illustrating a portion of the prior art wafer level IC test system of FIG. **3**,

FIG. **4** is a simplified side elevation view of a wafer level IC test system in accordance with an exemplary embodiment of the invention,

FIG. **5** is a block diagram of the wafer level IC test system of FIG. **4**,

FIG. **6** is a schematic and block diagram of a portion of the wafer level test system of FIG. **5**,

FIGS. **7–11** are schematic diagrams illustrating a portion of the wafer level test system of FIG. **5**,

FIGS. **12–14** illustrate alternative embodiments of the analog-to-digital converter of FIG. **6**,

FIG. **15** is a side elevation view of a probe assembly in accordance with an exemplary embodiment of the invention for providing signal paths between an integrated circuit tester to and a wafer, and

FIGS. **16–19** are schematic diagrams illustrating alternative versions of the signal paths provided by the probe assembly of FIG. **15**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

This specification describes one or more exemplary embodiments and/or applications of an invention considered by the applicant(s) to be the best modes of practicing the invention. However those of skill in the art will appreciate that there are other modes of practicing the invention, and there is no intention that the invention be limited to the particular embodiment(s) described below or to the manner in which the embodiments operate. The scope of the invention is defined by the claims appended to this specification.

The present invention relates to an apparatus for providing signal paths between an IC tester and terminals of ICs through which the ICs transmit and receive signals so that the tester can test the ICs. Some testers can test many ICs concurrently while they are still in the form of unseparated die on a semiconductor wafer. ICs typically include conductive pads on their surfaces that can act as terminals for receiving IC input signals from external circuits and for transmitting IC output signals to external circuits. While an interconnect system in accordance with an exemplary embodiment of the invention described herein below connects an IC tester to pads of ICs while still in the form of die on a semiconductor wafer, it should be understood that the invention could be employed to connect IC testers to pads of separated unpackaged ICs or to pins or other types of terminals of packaged ICs may also be adapted to employ the invention as described herein below.

FIGS. **4** and **5** illustrate an exemplary system **50** for testing a set of ICs **52** formed on a semiconductor wafer **54**. A set of coaxial cables **56** couple each channel **57** of an IC tester **58** to a connector **60** on the upper surface of a probe

card **62**. Probe card **62** provides signal paths linking the ends of conductors **56** at connector **60** to a set of probes **64**. Any type of probe card may be employed. Non-exclusive examples include a single printed circuit board (PCB) with probes attached directly to the PCB (as employed in exemplary system **50**) and probe card assemblies including several separate substrate layers interconnected by spring contacts or other means. Other non-exclusive examples of probe cards are disclosed in U.S. Pat. No. 5,974,662 issued Nov., 2, 1999 to Eldridge et al., and U.S. Pat. No. 6,064,213 issued May 16, 2000 to Khandros et al., each of which is incorporated herein by reference.

Various types of structures can be used to implement probes **64** including, for example, wire bond and lithographic spring contacts, needle probes, and cobra probes. When spring contacts are employed to implement probes **64**, they can be attached to pads formed on a lower side of probe card **62** and arranged so that their downward extending tips contact a set of pads **71** and **72** formed on the surfaces of ICs **52**. Spring contact probes **64** may alternatively be formed on pads **71** and **72** with tips of probes **64** extending upward to contact the pads formed on the lower surface of probe card **62**. Pads **71** and **72** may be the ICs' input/output (I/O) terminals or may be redistribution pads that are linked to the ICs' I/O terminals.

U.S. Pat. No. 6,064,213, issued May 16, 2000 to Khandros et al. (incorporated herein by reference) discloses an example of a card assembly designed to contact spring contacts formed on an IC. U.S. patent application Ser. No. 09/810,871 filed Mar. 16, 2001 (incorporated herein by reference) describes another example of a card assembly employing spring contact probes. U.S. Pat. No. 5,974,662 issued Nov. 2, 1999, issued to Eldridge et al., incorporated herein by reference, describes an example of a probe card assembly in which spring contacts formed on a probe card function as probes. The following documents (incorporated herein by reference) disclose various exemplary methods for manufacturing spring contacts: U.S. Pat. No. 6,333,269 issued Jan. 8, 2002 to Eldridge et al., U.S. Pat. No. 6,255,126 issued Jul. 31, 2001 to Mathieu et al., U.S. patent application Ser. No. 09/710,539 filed Nov. 9, 2000, and U.S. patent application Ser. No. 09/746,716 filed Dec. 22, 2000.

Tester **58** typically organizes a test into a succession of test cycles of uniform duration, and during each test cycle each tester channel **57** may generate an output test signal to be supplied to one or more of IC pads **71** and **72** or may receive an input signal having a voltage representing a logic state of IC output signals generated at pads **71** and **72**. Before starting a test, a host computer **63** supplies programming instructions to channels **57** via a bus **65** telling each channel **57** what to do during each test cycle.

Some of the pads **71** on the surface of a wafer **54** may act as IC input terminals that can only receive IC input signals generated by channels **57**. For example, the pads linked to control and address terminals of a RAM or of a read only memory (ROM) are uni-directional input terminals.

Other pads **72** on wafer **54** may act as uni-directional IC output terminals that can only produce IC output signals at the pads or as bi-directional input/output terminals that can both transmit and receive signals. For example, pads linked to data terminals of a ROM are uni-directional output pads whereas the pads linked to data terminals of a RAM are bi-directional I/O pads.

If tester **58** were to include a separate tester channel **57** for each pad **71** or **72**, probe card **62** could provide a separate signal path **68** between each pad **71** or **72** and its corresponding tester channel **57**. For example ICs **52** might be RAMs for storing 8-bit data at 8-bit addresses. The RAMs could be tested by writing data to each address and then reading the data back out to determine whether it matches the data written into that address. Each RAM would have eight input pads **71** for receiving an address, eight I/O pads **72** for transmitting and receiving data, and, for example, two input pads **71** for receiving control signals. If probe card **62** were to connect only one pad to each channel **57**, IC tester **58** would have to provide 18 channels **57** for each RAM to be tested. If wafer **54** contained 100 RAMS, then tester **58** would have to have 1800 channels in order to test all RAMs concurrently.

Since all ICs **52** formed on wafer **54** are usually similar and are tested in the same way and at the same time, each IC **52** would receive the same set of input address and control signals during any given test cycle. To reduce the number of tester channels **57** needed, probe card **62** provides a set of branching signal paths **74**, each for linking one tester channel **57** to more than one IC input pad **71**. For example, when the ICs **52** being tested are RAMs having 8-bit input addresses A0–A7, probe card **62** delivers an output signal of one tester channel **57** as the A0 address input to each of multiple (N) RAMs, seven other tester channels **57** supply the A1–A7 address bits to the same set of N RAMs. Thus only eight channels **57**, rather than 8*N channels, are needed to supply an 8-bit address to each of N RAMs. Similarly branched paths **74** may be provided to deliver a control signal produced by one channel **57** to inputs pads of N RAMs.

Various faults can occur at any input pad **71**. For example a pad **71** may be shorted through a low impedance path to ground, to a power source, or to a nearby signal pad **71** or **72**. Each branch of a signal path **74** delivering an input signal to more than one IC input pad **71** includes an isolation resistor **75**. All resistors **75** in paths **74** linked to uni-directional input pads **71** may be of similar or differing resistance, however all isolation resistors **75** are of sufficient size that a fault at any one IC input pad **71** will not substantially influence the voltage of the channel output signal VOUT supplied to any other IC input pad **71** through the same path **74**.

Probe card **62** also provides another set of branching signal paths **76**, each linking a set of N IC output or I/O pads **72** to the same circuit node **84** within the probe card. When pads **72** are to receive input signals, a single tester channel **57** supplies the same input signal to all N pads **72** via the branching path **76**. When pads **72** are to produce output signals, a signal developed at node **84** of path **76** in response to the N IC output signals produced at pads **72** is supplied as an input signal to a single tester channel **57**.

Each i^{th} branch of an N-branch signal path **76** includes a scaling resistor **77** of magnitude R_i. The scaling resistors **77** in the branches of any signal path **76** are all of differing resistances so that the voltage of the signal developed at node **84** depends on the combination of logic states of all of the IC output signals produced at the N output pads **72** linked to node **84**. Assuming the N IC output signals form an N-bit binary number, then with values of resistors **77** appropriately chosen, the voltage of the signal developed at node **84** will be a monotonic function of the value of that binary number. When a tester channel **57** measures the voltage of the signal developed at one of nodes **84** with sufficient resolution, it is possible to determine the logic state of each of the N signal produced at the IC output pads **72** that are linked to that node.

FIG. **6** shows a set of N drivers **80** within ICs formed on wafer **54** generating a set of N output signals V_1–V_N

produced at IC output pads **72**. Probes **64** deliver output signals V_1–V_N to a set of pads **82** on the lower surface of probe card **62**. Probe card **62** provides a branching path **76** including scaling resistors R_1–R_N for linking pads **82** to a common node **84**. A coaxial cable **56** links node **84** to an input terminal **86** of a tester channel **57**. When coaxial cable **56** has a characteristic impedance of, for example 50 Ohms, an optional 50 Ohm resistor RIN may be provided within tester channel **57** to terminate the coaxial cable when necessary to eliminate signal reflections at terminal **86**. Termination resistor RIN may not be needed in applications where such signal reflections are not problematic.

Tester channel **57** includes an analog-to-digital converter (ADC) **88** for receiving the VIN signal and for producing M-bit thermometer code output data (DATA). Each of the M+1 possible values of DATA represents a different voltage range. The current value of DATA indicates the particular range within which the voltage of the ADC's VIN input signal resides. Each tester channel **57** also includes a data acquisition and control circuit **90** supplying reference data DREF as input to ADC **88** for controlling the relationship between each value of DATA and the voltage range it represents.

Circuit **90** also samples the value of the DATA output of ADC **88** at a time during each test cycle at which the V_1–V_N signals are expected to stabilize at their expected logic levels. Before starting a test, host computer **63** of FIG. **5** programs circuit **90** with instructions supplied via bus **66** telling it how to adjust the range of ADC **88** and indicating times during each test cycle at which the DATA value is to be sampled. In one embodiment of the invention, circuit **90** stores the sampled value of DATA for each test cycle so that host computer **63** (FIG. **5**) can thereafter read the sampled DATA value to determine the voltage of the VIN signal produced during each cycle of the test. This enables the host computer to determine the logic state of each IC output signal V_1–V_N during each test cycle. Alternatively, the instructions that the host computer supplies to control circuit **90** before the start of the test may indicate expected values of the DATA output of ADC **88** for each test cycle. Circuit **90** then determines from DATA value acquired during each test cycle whether any output signal V_1–V_N is of an incorrect state during any test cycle.

Assume, for example, that N=2, so that probe card **62** links two IC output pads **72** to the input **86** of one tester channel **57**. Assume also that the nominal low and high logic levels for each output signal V_1–V_N are 0 and 5 volts, the output impedance of each driver **80** is much lower than 50 Ohms, and the input impedance of ADC **88** is much higher than 50 Ohms. Further, assume as depicted in FIGS. **7**–**10** that RIN=50 Ohms, R_1=50 Ohms, and R_2=25 Ohms. Then as illustrated in FIG. **7**, when both V_1 and V_2 are 0 volts, VIN will be 0 volts. As illustrated in FIG. **8**, when both V_1 and V_2 are 5 volts, VIN will be 3 volts. FIG. **9** shows that when V_1 is 0 volts and V_2 is 5 volts, VIN will be 2.5 volts. As seen in FIG. **10**, when V_1 is 5 volts and V_2 is 0 volts, VIN will be 2 volts. Table I summarizes the relationships between voltage magnitudes of V_1, V_2 and VIN.

TABLE I

V_2	V_1	VIN
0	0	0
0	5	2
5	0	2.5
5	5	3

Since VIN may be of any of four different voltage levels depending on the logic states of the V_1 and V_2 signals, it is possible to determine the logic state of each signal when ADC **88** is able measure the voltage of VIN with sufficient resolution. When M=3, ADC **88** produces a 3-bit output thermometer code DATA which can represent any of four voltage ranges. In such case circuit **90** may, for example, set the DREF data input to ADC **88** so that ADC **88** responds to values of VIN in the ranges indicated in TABLE II by producing the indicated values of the 3-bit thermometer code DATA.

TABLE II

VIN	DATA
VIN < 1.75	000
1.75 V < VIN < 2.25 V	001
2.25 V < VIN < 2.75 V	011
2.75 V < VIN	111

With these ADC settings, the data input to data acquisition and control circuit **90** distinguishes from among the four possible voltage levels of the VIN signal and therefore enables circuit **90** or the host computer to determine the logic state each of the IC output signals V_1 and V_2 from which the VIN signal is derived.

FIG. **11** illustrates an example in which N=3 such that probe card **62** of FIG. **6** links the output pads **72** of three ICs **52** to the input terminal of a single tester channel **57**. Assume again that the low and high logic levels of the IC output signals V_1–V_3 produced at the three IC output pads **72** are 0 and 5 volts and that the input impedance of ADC **88** is very high, and the output impedance of drivers **80** is very low. In this example we assume signal reflections at terminal **86** of channel **57** are not problematic and that no resistor RIN is needed to terminate coaxial cable **56** with its characteristic impedance.

As illustrated in FIG. **11** we can, for example, set R_1=100 Ohm, R_2=50 Ohms and R_3=25 Ohms. Table III below illustrates the possible combinations of V_1–V_3 voltages and the VIN voltage resulting from each combination:

TABLE III

V_3	V_2	V_1	VIN
0	0	0	0
0	0	5	0.71
0	5	0	1.43
0	5	5	2.14
5	0	0	2.86
5	0	5	3.57
5	5	0	4.29
5	5	5	5

When ADC **88** is capable of producing a 7-bit output thermometer code DATA, circuit **90** may, for example, set ADC **88** to respond to values of VIN in the ranges indicated in TABLE IV below by producing the indicated values of thermometer code DATA.

TABLE IV

VIN	DATA
VIN < .35 V	0000000
.35 v < VIN < 1.05 V	0000001
1.05 V < VIN < 1.75 V	0000011
1.75 V < VIN < 2.50 V	0000111
2.50 V < VIN < 3.20 V	0001111
3.20 V < VIN < 3.90 V	0011111
3.90 V < VIN < 4.65 V	0111111
4.65 V < VIN	1111111

In general, when probe card **62** employs a set of N scaling resistors R_1–R_N of appropriately dissimilar resistances to combine the output signals V_1–V_N of a set of N IC output pads **72** to form a single signal input VIN to ADC **88**, the various combinations of V_1–V_N logic states may drive the VIN signal to any of 2^N voltage levels. In order to enable data acquisition and control circuit **90** or a host computer to distinguish from among the 2^N VIN possible voltage levels, and therefore to determine the logic state of each signal V_1–V_N, the DATA output of ADC **88** is preferably at least $M=2^N-1$ bits wide, and the voltage ranges represented by each value of DATA must be appropriately selected.

However as illustrated in FIG. **3**, a channel **24** of a prior art IC tester to be employed in this application may have, for example, only two comparators **38** and **39**. Such a tester channel **24** can compare a VIN signal to only two reference levels VH and VL produced by a pair of digital-to-analog converts (DACs) **40** and **41**. Thus comparators **38** and **39** and DACs **40** and **41** can act as an ADC capable of producing only a 2-bit thermometer code {CH, CL} representing the voltage level of the VIN signal as residing within one of only three ranges. Tester channels in some prior art IC testers include only a single comparator acting as a single-bit ADC that can distinguish between only two voltage ranges.

When a probe card in accordance with an exemplary embodiment of the invention combines multiple (N) IC output signals in the manner described above to produce a VIN signal input to a tester channel having only one or two comparators, the channel's 1 or 2 bit comparator output does not represent the voltage of the VIN signal with sufficient resolution to enable a host computer to determine the state of each of the N IC output signal V_1–V_N. Nonetheless, it is possible to use a conventional tester channel producing only a 1-bit or 2-bit thermometer code output (i.e. M<3) to monitor a VIN signal representing multiple IC output signals V_1–V_N, and yet provide sufficient information to enable the host computer to determine the state of all signals V_1–V_N during each test cycle.

One way to do that is perform the same test on the ICs several times, with the comparator reference voltages being set to different values during each repetition of the test. For example, assume that three IC output signals V_1–V_3 having low and high states of 0 volt and 5 volts are combined as illustrated in FIG. **11** to provide a single VIN input to a tester channel having only a single comparator. Thus, referring to FIG. **6**, N is 3 and M is 1. VIN could be of any of 8 levels as illustrated in Table III above. Since the ADC output DATA has only a single bit and can only represent two VIN voltage ranges and not eight, data acquisition and control circuit **90** is programmed to run the test seven times. For example, referring to Table IV above, during all cycles of the first repetition of the test, ADC **88** is set to drive the single-bit DATA to a 1 when VIN exceeds 0.35 volts. During all cycles of the second repetition of the test, ADC is set to drive DATA to a 1 only when VIN exceeds 1.05 volts. During the third through the seventh repetitions of the test, ADC is set to drive DATA to a 1 when VIN exceeds 1.05V, 1.75V, 2.50V, 3.20 v, 3.90V, and 4.65V, respectively. The seven bits of data acquired during the Kth cycle of each of the seven repetitions of the test will enable the host computer **63** to determine the state of each signal V_1–V_3 during that Kth test cycle.

When data acquisition and control circuit **90** is capable of adjusting the DREF input to ADC **88** at the start of each test cycle (rather than only at the start of each test), test cycles in which the IC's output signals states are to be determined can be repeated 7 times using a different value of DREF for each repetition. For example when a single tester channel is monitoring data bit outputs V_1–V_3 of a ROM IC, the ROM's address inputs are kept the same for seven test cycles so that each ROM continues to read out data at the same address for seven test cycles. However DREF is set to a different value for each of the seven cycles so that the state of each bit V_1–V_3 can be determined from the sequence of seven DATA bits produced during those seven test cycle.

Increasing the number M of bits in the DATA output of ADC **88** decreases the number of times each data read cycle must be repeated in order to gather a sufficient amount of data to determine the voltage level of each of the combined IC output signals. For example a tester channel having two comparators acting as an ADC **88** producing a 2-bit (M=2) output DATA could be used to monitor a VIN signal representing the combination of three IC output signals V_1–V_3 if each test cycle were repeated four times, with the DREF data being appropriately adjusted prior to each test repetition.

The M-bit ADC **88** of FIG. **6** may have any of a variety of architectures. FIG. **12** illustrates an exemplary ADC having M comparator units **94**(**1**)–**94**(M), each including a comparator **95** and a DAC **96**. The DAC **96** of each comparator unit **94** converts a separate field of the DREF data into a reference voltage VREF. The comparator **95** of each unit **94** compares the VIN signal to reference voltage VREF to produce a separate bit of M-bit output DATA.

FIG. **13** illustrates another suitable architecture for ADC **88** of FIG. **6**. Selected values of the DREF data are written into successive addresses of a RAM **100** addressed by the output ADDR of a counter **102**. A DAC **104** converts data read out of RAM **100** into a reference voltage VREF supplied as input to a comparator **106** which compares VREF to VIN and asserts its output COMP when VREF is higher in voltage than VIN. A leading edge of the COMP output of comparator **106** clocks a register **108** which stores the ADDR output of counter **102**. Register **108** supplies its contents as the ADC's DATA output. A START signal pulse supplied by circuit **90** of FIG. **6** marks a point during each test cycle at which the VIN data is expected to stabilize to a high or logic level. The START signal resets the counter's ADDR output to 0, and thereafter counter **102** increments its ADDR output on each pulse of a clock signal CLK so that RAM **100** successively reads out DREF data stored at successive RAM addresses. DAC **104** responds to the continuously increasing DREF data by continuously increasing the VREF input to comparator **106**. When VREF exceeds VIN, comparator **106** asserts the COMP signal causing register **108** to store the current ADDR output of counter **102**. Thus by the time counter **102** has reached its count limit during the test cycle, register **108** will have stored the ADDR value resulting in the lowest VREF voltage that exceeds VIN. In this version of ADC **88**, the DATA value can appear in binary-encoded form rather than in thermometer code

form. With the DREF data stored in RAM **100** providing a sufficient number of appropriately adjusted VREF levels, a host computer can determine the V_1–V_N signal states from the DATA output of register **108**.

FIG. **14** illustrates a version of ADC **88** of FIG. **6** suitable for use in a tester that is customized to test a particular kind of IC. In such case, the reference voltage levels represented by the various values of DATA need not be adjustable. The ADC of FIG. **14** includes a resistor network **110** dividing a supply voltage VDD to produce a set of reference voltages VREF(1)–VREF(M) supplied as input to a set of M comparators **112**(1)–**112**(M). Each comparator **112** compares its input reference voltage to VIN to produce a separate bit of the ADC's output DATA.

FIG. **15** illustrates another exemplary embodiment of the invention, a multiple-layer probe card assembly **120** for providing signal paths between an integrated circuit tester **122** and pads **123** on surfaces of IC dice **124** on a wafer **126** under test. Probe card assembly **120** includes a probe board **130** having a set of pads **132** on its upper surface for receiving tips of a set of pogo pin connectors **134** providing signal paths between tester **122** and pads **132**. An interposer layer **135** having a set of spring contacts **136** and **138** connected to its upper and lower surfaces provides signal paths between a set of contacts **140** on the lower surface of probe board **130** and a set of contacts **142** on an upper surface of a space transformer board **144**. A set of probes **146** provide signal paths between pads **148** on the lower surface of space transformer **144** and IC pads **123**. Probe board **130**, interposer **138** and space transformer **144** may include single or multiple insulating substrates with traces formed on the substrates and vias extending through the substrate for conducting signals horizontally and vertically between pads and/or contacts on their upper and lower surfaces.

In accordance with this exemplary embodiment of the invention, some of the signal paths though probe board assembly **120** branch so that a channel of IC tester **122** employing a single one of pogo pins **134** as an input and/or output terminal can concurrently access more than one IC pad **123**. Isolation resistors (not shown in FIG. **15**) formed on or within one or more of layers **130**, **135** and **144** are included in the branching paths between pogo pins **134** and IC pads **123**.

FIGS. **16**–**19** are schematic diagrams illustrating various alternative versions of a branching signal path within probe board assembly **120**. In FIG. **16** the isolation resistors **150** are formed on or between layers of probe board **130**. In the versions of FIGS. **17** and **18**, the isolation resistors **150** are formed on or between layers of interposer **135** and space transformer **134**. A hierarchical resistor network may also be implemented by mounting resistors on one or more boards of probe board assembly **120**. For example, FIG. **19** illustrates a signal path including a hierarchy of isolation resistors **150** formed on probe board **130** and on space transformer **134**. Resistors **150** may be of suitably differing values as described above when one tester channel is to monitor IC output signals at more than one IC pad **123**.

Thus has been shown and described a probe card for providing signal paths between IC tester channels and input and output pads the surfaces of ICs formed on a semiconductor wafer wherein some of the paths link one tester channel to more than one input or output pad. The forgoing specification and the drawings depict the best modes of practicing the invention, and elements or steps of the depicted best modes exemplify the elements or steps of the invention as recited in the appended claims. However the appended claims are intended to apply to any mode of practicing the invention comprising the combination of elements or steps as described in any one of the claims, including elements or steps that are functional equivalents of the example elements or steps depicted in the specification and drawings.

What is claimed is:

1. An apparatus for providing signal paths between integrated circuit (IC) tester channels and input and output pads residing on surfaces of a plurality of ICs, wherein the ICs are adapted to receive test signals via the input pads and to generate output signals at the output pads in response to the test signals, and wherein voltages of the test signals and the output signals represent logic states, the apparatus comprising:

a first node; and

N first signal paths,

wherein N is an integer greater than one,

wherein each first signal path links a separate one of the output pads to the first node, such that a first signal is produced at the first node in response to a set of N output signals generated at the output pads linked to the first node, and

wherein all N first signal paths have substantially differing resistances such that a voltage of the first signal has a unique magnitude for each unique combination of logic states of the set of N output signals.

2. The apparatus in accordance with claim **1** further comprising first conductive means for delivering the first signal appearing at the first node as an input signal to one of the IC tester channels.

3. The apparatus in accordance with claim **1** further comprising:

a second circuit node;

a plurality of second signal paths, each corresponding to a separate one of the IC input pads and delivering a test signal from the second circuit node to the corresponding IC input pad, wherein each second signal path is of sufficient resistance that a short linking the corresponding IC input pad to any source of potential within the IC upon which the IC input pad resides would not alter the logic state of the test signal at the second circuit node.

4. The apparatus in accordance with claim **3** further comprising:

first conductive means for delivering the first signal appearing at the first node as an input signal to one of the IC tester channels, and

second conductive means for delivering a test signal produced by another of said tester channels to the second circuit node.

5. An apparatus for providing signal paths between integrated circuit (IC) tester channels and input pads and output pads residing on surfaces of a plurality of ICs, wherein the ICs are adapted to receive test signals via the input pads and to generate output signals at the output pads in response to the test signals, and wherein voltages of the test signals and the output signals represent logic states, the apparatus comprising:

at least one substrate having a surface;

a first circuit node formed on said at least one substrate;

N first conductive pads formed on said surface, where N is an integer greater than 1;

N first probes, each first probe linking a separate one of N of said output pads to a corresponding one of the N first conductive pads; and

N first signal paths, each linking a corresponding one of the N first conductive pads to said first circuit node such that a first signal is produced at the first circuit node in response to a set of N output signals generated at the output pads linked to the first circuit node, all N first signal paths have substantially differing resistances such that a voltage of the first signal has a unique magnitude for each unique combination of logic states of the set of N output signals.

6. The apparatus in accordance with claim **5** wherein portions of the N first signal paths are formed on said at least one substrate.

7. The apparatus in accordance with claim **5** wherein said at least one substrate comprises:

a first substrate having said surface; and

a second substrate, spaced from said first substrate, said first circuit node being formed on said second substrate, wherein said first signal paths are formed on and extend between the first and second substrates.

8. The apparatus in accordance with claim **5** where said at least one substrate comprises:

a first substrate having said surface; and

a second substrate, spaced from said first substrate, said first circuit node being formed on said second substrate; and

a third substrate residing between and spaced from said first and second substrates, wherein said first signal paths are formed on and extend between the first, second and third substrates.

9. The apparatus in accordance with claim **5** further comprising first conductive means for delivering the first signal appearing at the first circuit node as an input signal to one of the IC tester channels.

10. The apparatus in accordance with claim **5** wherein each first probe comprises a spring contact.

11. The apparatus in accordance with claim **5** wherein the apparatus further comprises:

a second circuit node formed on the substrate;

a plurality of second conductive pads formed on the surface of the substrate;

a plurality of second probes, each second probe linking a separate one said input pads to a corresponding one of the plurality of second conductive pads; and

a plurality of second signal paths, each corresponding to a separate one of the second conductive pads for delivering a test signal applied to the second circuit node to the corresponding second conductive contact, wherein each second signal path has substantial resistance sufficient to prevent a fault at any of the inputs pads from affecting a logic state of the test signal applied at the second circuit node.

12. The apparatus in accordance with claim **11** further comprising:

first conductive means for delivering the first signal appearing at the first circuit node as an input signal to one of the IC tester channels, and

second conductive means for delivering a test signal produced by another of said tester channels to the second circuit node.

13. The apparatus in accordance with claim **12** wherein each first probe and each second probe comprises a spring contact.

14. An apparatus for testing integrated circuit (ICs), wherein the ICs have input pads at which the ICs receive test signals, and have output pads at which they produce output signals in response to the test signals, the test and output signals having voltages representing logic states, the apparatus comprising:

a first circuit node;

N first signal paths, wherein N is an integer greater than one, wherein each first signal path links a separate one of the output pads to the first circuit node, and wherein each first signal path has a resistance differing substantially from a resistance of any other of the first signal paths, such that a first signal appears at the first circuit node having a first voltage representing a combination of logic states of the output signals produced by the output pads linked by the first signal paths to the first circuit node; and

a first IC tester channel linked to the first circuit node including means for measuring the first voltage of the first signal.

15. The apparatus in accordance with claim **14** wherein the means for measuring the first voltage of the first signal comprises an analog-to-digital converter (ADC) for generating output data in response to the first signal, wherein a value of the output data represents a voltage range in which said first voltage resides.

16. The apparatus in accordance with claim **15** wherein the ADC comprises:

a digital-to-analog converter (DAC) for generating a reference voltage of magnitude determined by a value of control data supplied as input to the DAC; and

a comparator receiving the reference voltage and the first signal for generating an output bit indicating whether the first voltage is greater than the reference voltage.

17. The apparatus in accordance with claim **16** wherein the ADC further comprises means for periodically altering the value of the control data.

18. The apparatus in accordance with claim **15** wherein the ADC comprises:

means for generating M reference voltages, of substantially differing magnitudes, where M is an integer greater than 1, and

M comparators, each comparator corresponding to a separate one of the M reference voltages, each comparator receiving its corresponding reference voltage and the first signal as inputs, and each comparator generating a separate bit of an M-bit data word, wherein the bit generated by each comparator indicates whether the first voltage is greater than its corresponding reference voltage.

19. The apparatus in accordance with claim **18** wherein M is at least as large as 2^N-1 and wherein the magnitudes of said M reference voltages are such that each possible combination of logic states of the output signals produced by the output pads linked by the first signal paths to the first circuit node results in a unique value of the M-bit data word.

20. A method for testing at least one integrated circuit (IC) device wherein at least one IC device comprises a plurality of terminals at which said at least one IC device receives input signals and concurrently produces output signals, wherein voltages of the input and output signals represent logic states, the method comprising the steps of:

a. providing a first circuit node;

b. providing a plurality of first signal paths, each first signal path linking a separate one of the plurality of terminals to the first circuit node, such that a first signal is produced at the first circuit node in response to IC output signals concurrently generated at each of the plurality of IC terminals, wherein all first signal paths

have substantially differing resistances such that a voltage of the first signal produced at the first circuit node has a unique magnitude for each unique combination of logic states of the IC output signals produced at the plurality of IC terminals;

c. measuring a voltage of the first signal produced at the first circuit node; and

d. determining a logic state of each of the plurality of output signals from the voltage measured at step c.

21. The method in accordance with claim **20** further comprising the step of:

e. applying a test signal to the first circuit node such that the test signal travels from the first circuit node to each of the plurality of IC terminals via a separate one of the first signal paths, such that the test signal becomes an input signal received by each of the plurality of IC terminals.

* * * * *

EXHIBIT K

Exhibit Designated

HIGHLY CONFIDENTIAL ATTORNEYS' EYES ONLY

Under Stipulated Protective Order